Enabling System-Level Debug
Merging Software and Hardware Debug Infrastructures to Accelerate the Post-Silicon Validation of SoCs

Brad Quinton, Ph.D.
Chief Architect, Embedded Instruments
Tektronix
Embedded Instrumentation

- The system is moving on-chip.....

.....but, system observability is lost!
Embedded Instrumentation

- **Solution**: move the instruments on-chip too!

- Embedded instruments:
  - Operate at-speed (800 MHz+)
  - Scale with underlying IC technology
  - Enable very wide captures (1024+ bits wide)
  - Don’t consume valuable I/O resources
  - Can be applied *any* level in the design (from internal state machines to the system bus to the PHY)
  - Naturally handle different clock domains
  - Are available in-system, even in the field!
Tektronix acquires Veridae Systems Inc. and forms Tektronix Embedded Instrumentation Group:

Tektronix buys validation tool vendor
7/5/2011 8:19 PM EDT
NEW YORK—Test and measurement vendor Tektronix Inc. Tuesday (July 5) announced the acquisition of ASIC/FPGA prototyping debug software provider Veridae Systems Inc. Terms of the acquisition were not disclosed.

Veridae (Vancouver, Canada) was founded in 2009 to commercialize research from the University of British Columbia. The firm sells three tools for ASIC/FPGA prototyping debug, ASIC post silicon validation and FPGA-based system product validation into semiconductor and system product companies.
There is nowhere to hide...:

- Multiple cores
- Heterogeneous cores
- Integrated memory controllers
- Integrated high-speed I/O
- Complex cache structures
- Video / Encryption off-load
- Etc.

There are no more “stand-alone” processors, no more “simple software”. It is an SoC world...
Productivity Gap

- Key behaviors now span software and hardware
- Functional complexity is high and growing
- Most interfaces are now “hidden”
- Teams are large and diverse
- Bring-up, validation, debug, are all taking longer and more resources

“… a radical transformation is necessary if [post-silicon] validation is to be effective in the near future.”

- P. Patra, Senior Staff Scientist, Intel

Baseline SoC: Functionality Across Abstract Layers

Software Execution

Transaction Flow

Protocol Decode

Transmitter/R

Physical Layer
Key issue to determining root-cause:

What is the causal relationship between behaviors that cross hardware and software?

i.e. Did the software fail because of the hardware; or the other way around? Who was wrong first? How do we make sense of these results together?
Integrated Event Management: Merging HW/SW Debug

Software Debug

Hardware Debug Infrastructure

Subsystem 1

Capture Station

Subsystem 2

Subsystem n

JTAG

TAP Controller

Access Control

Local CPU

S/W Debug Infrastructure

Simple Router

Integrated Event Management
Case 1: Software is executing an unexpected area of the code
Action: Software breakpoint causes hardware trigger
**Case 2:** Hardware is not processing the data as expected.

**Action:** Hardware trigger causes software breakpoint
Conclusion

- It is possible to achieve *single event* synchronization around both software and hardware debug events.
- Allows for the meaningful presentation of **simultaneous** debug data from both infrastructures.
- We believe this *full system view* is critical to effective SoC debug.
- See this example running live at the Tektronix DAC booth (302) ....