

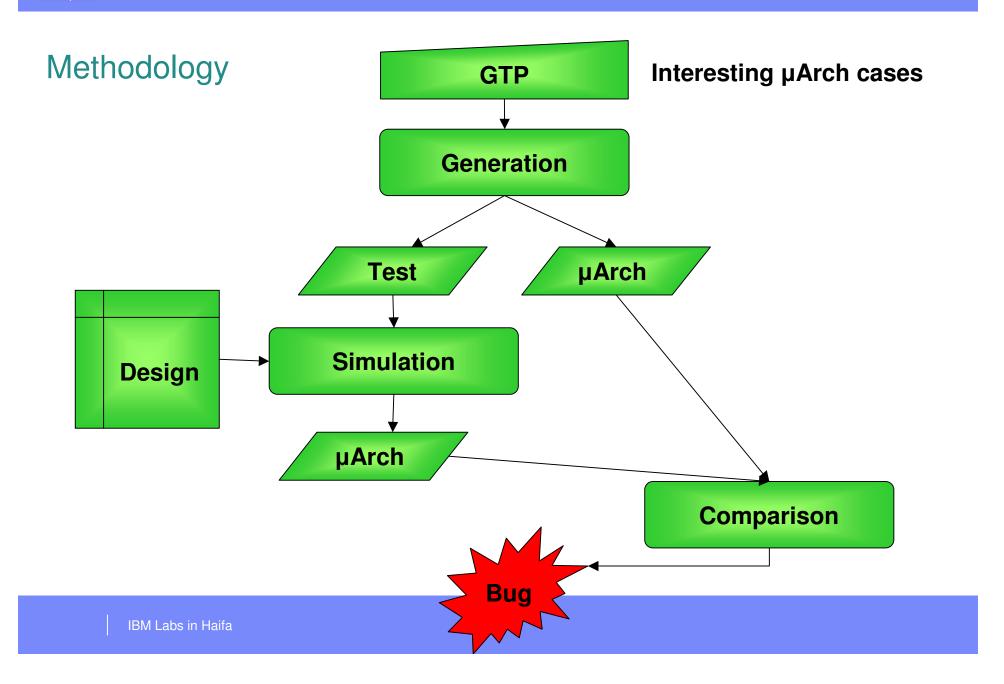
Piparazzi: A Test Program Generator for Micro-architecture Flow Verification

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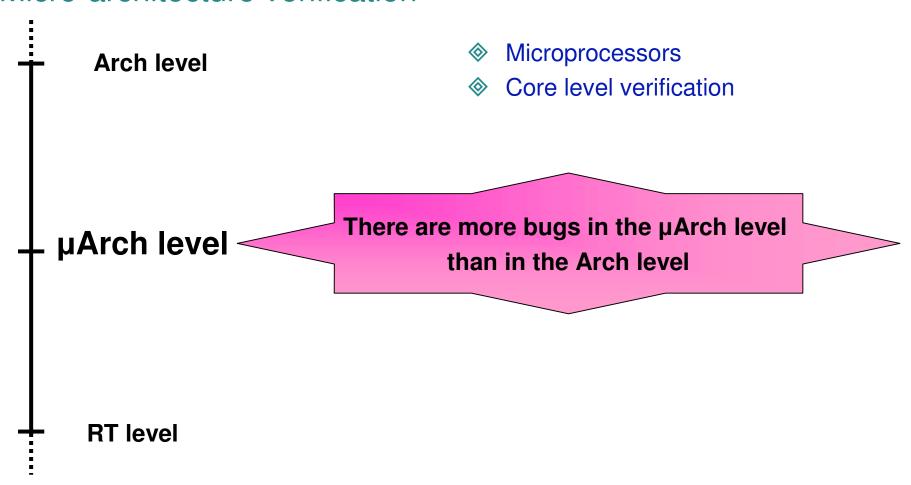


Outline

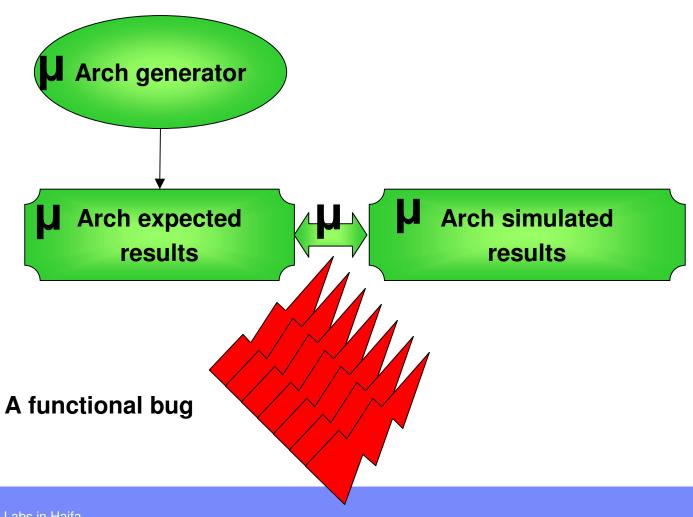
- Methodology
- ♦ Types of bugs
- ♦ Generic Test Plan (GTP)
- Generation
- Results and summary



Micro-architecture verification

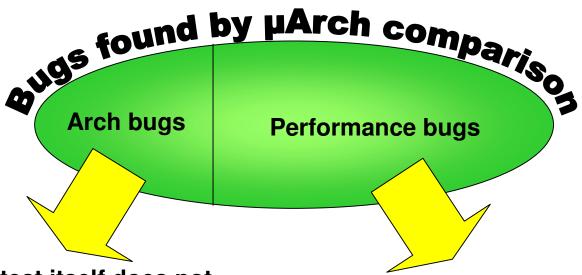


Different abstraction levels to find a **functional** bug using expected results



Classification of bugs found by **µArch** comparison

Bugs found by μArch discrepancy: timing, mechanism, location

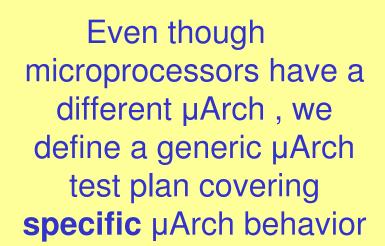


While the test itself does not show a functional problem, it can be inferred from an analysis of the faulty µArch behavior

Cannot be found by arch comparison

Generic Test Plan – processor independent test plan

- Coverage models for different units in the processor
- Cross-product coverage models
- Coverage models for resources and instructions
- ♦ Knowledge reuse





An example

For each pipeline in the processor

For each stage in the pipeline

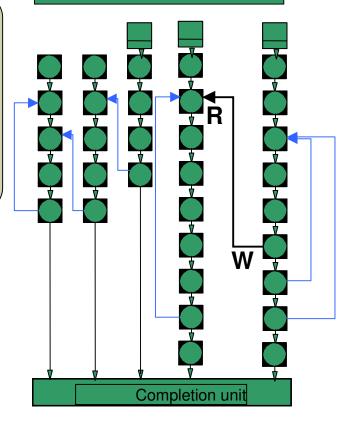
For each stall reason in the stage

Generate a test that creates the stall

Fetch unit

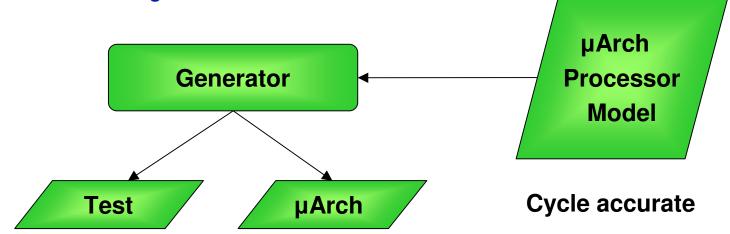
Decode unit

Dispatch unit



Generator

- Model-based (processor independent)
- Based on CSP
- Coverage by generation
- Two main outputs
- Slower than random test generator



µArch model

- Enables the definition of different microprocessors
 (Out of order, Pipelines, Super scalar, Multithreading)
- A cycle accurate model

Modeling

■ Configuration of predefined building blocks

Types of building blocks

Hardware

Fetch
Dispatcher
Pipeline
Cache
Branch prediction
Queue

Mechanisms

Flush
Forwarding
Interrupt
Splitting instruction

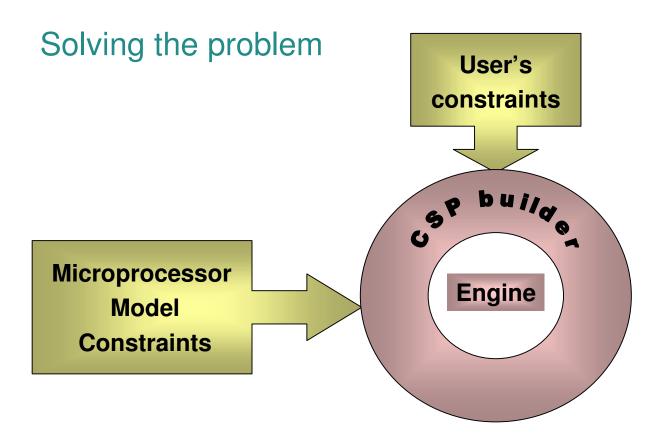
Instructions

add sub load store sync

The model:

Each BB may have variables, constraints, parameters, and BBs





csp builde,

Each building block creates its modeled CSP variables Each building block inserts its constraints:

Design independent constraints

Design dependent constraints (modeled)

User's constraints are inserted



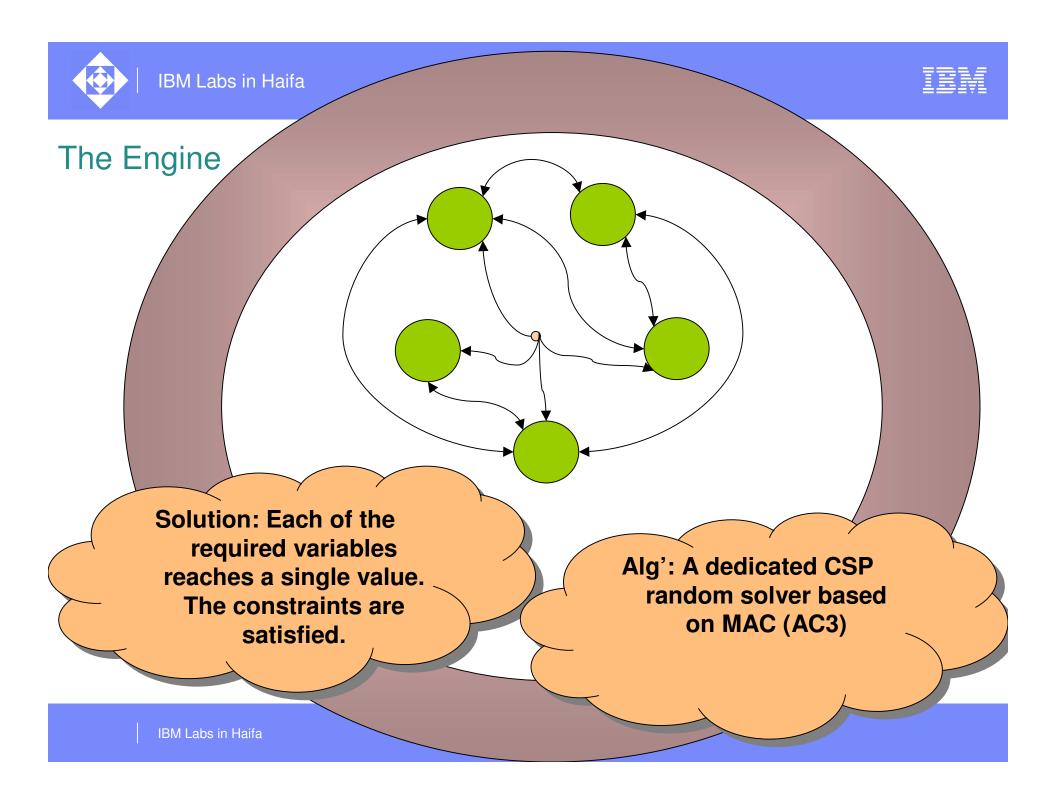
Fet

Deco

Dispa

Example for constraints: pipeline stage building block

- Design independent constraints:
 - **♦ EXIT = ENTRY + TOTAL_STALL**
 - **♦ TOTAL_STALL = SELF_STALL+...**
- Design dependent constraints:
 - The conditions and amounts for an instruction to be stalled in the stage (SELF_STALL)
 - **The rules for grouping instructions in the stage**
 - The conditions and timing to stall the stage above this one based on the instruction in this stage



Maintain Arc Consistency AC3

- 1. Bring every arc to a consistent state (if empty set -> backtrack)
- 2. Choose a variable (if none -> success)
- Choose a Value (if none -> backtrack (back jumping))
- 4. Go to 1

A = B + C

A =
$$\{1, 2, 3, 4, 6, 6\}$$

B = $\{3, 7\}$

C = $\{0, 3\}$

Specific issues for big and intricate CSPs

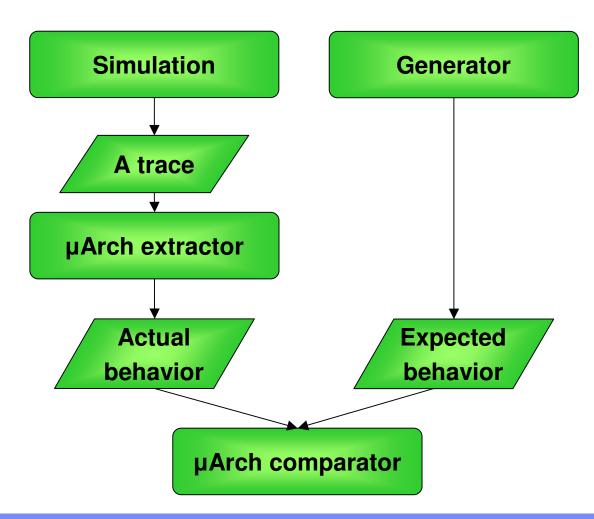
- Insert constraints on-the-fly just when necessary
- Different techniques to improve consistency for better success rate
- Domain specific heuristics for variable ordering
- Massive sharing of sub-constraints
- Domain specific redundant constraints



More backtracks

More time on consistency

µArch comparison



Results

- Working with mainstream high-end IBM processors
- We found many bugs; most of them by using µArch comparison
- ♦ About ¾ of the bugs are performance bugs
- Experiment results: Many interesting μArch events have a very low chance of being hit by random test generator (non-μArch)
- ♦ It is usually not easy to find a test that reveals the architectural bug based on a µArch discrepancy

Summary

- Bugs have difficulty remaining underground when covering a comprehensive µArch test plan

"Language shapes the way we think, and determines what we can think about" - B.L.Whorf