IBM HAIFA LABS

Invitation to IBM's Compiler and Architecture Seminar 2003

November 11, 2003

Organized by IBM Research Lab in Haifa, Israel

http://www.haifa.il.ibm.com/Workshops/compiler2003/index.html

Following last year's success, the Software and Verification Department at the IBM Haifa Research Lab (HRL) cordially invites you to a full-day seminar on compiler optimization and computer architecture, to be held on Tuesday, November 11, 2003. The seminar will take place at HRL's site on the Haifa University campus, in the HRL auditorium (room L100), from 9:15 to 17:15. Lunch and light refreshments will be served. Participation is free. The official language of the workshop is English.

9:15 Arrival

9:30 *Welcome*
David Bernstein, Mgr., Software and Verification Technologies, IBM Haifa Labs

9:45 *EXPRESS: A Rapid Prototyping/Development Environment for Embedded Computer Systems*
Alex Nicolau, University of California, Irvine

10:25 *Data Cache Design and Evaluation for SMT Processors*
Ron Pinter and Haggai Yedidya, Technion

10:55 *Subsetting SPEC When Measuring Results: Research vs. Industry*
Daniel Citron, IBM Haifa Labs

11:25 Coffee break

11:45 *Schemes for the Efficient Concurrent Use of Multiple Prefetchers*
Alex Gendler, Avi Mendelson, and Yitzhak Birk, EE Department, Technion, and Intel Haifa

12:15 *Power Awareness through Selective Dynamically-Optimized Traces*
Roni Rosner, Yoav Almog, Naftali Schwartz, Avi Mendelson, Micha Moffie, Ari Schmorak and Ronny Ronen, Microprocessor Research, Intel Labs, Haifa

12:45 *Static Detection of Thread Local Storage in C*
Yair Sade and Mooly Sagiv, Tel Aviv University

13:15 Lunch

14:20 Keynote: *Kilo-instructions Processors*
Mateo Valero, Universidad Politecnica de Catalunya (UPC), Spain

15:10 *JavaSplit: A Runtime for Execution of Monolithic Java Programs on Heterogeneous Collections of Commodity Workstations*
Assaf Schuster, Konstantin Shagin, and Michael Factor, Technion and IBM Haifa Labs

15:40 Break

16:00 *Choosing Among Alternative Pasts*
Marina Biberstein, Shmuel Ur, and Eitan Farchi, IBM Haifa Labs

16:30 *Overlapping Memory Operations with Circuit Evaluation in Hardware Compilation*
Yosi Ben-Asher, Haifa University, and Gad Haber, IBM Haifa Labs

17:00 *Concluding Remarks*
Bilha Mendelson, Manager - Code Optimization Technologies, IBM Haifa Research Lab

ORGANIZING COMMITTEE

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IBM Research Lab in Haifa