

Invited Talk

Fear, Uncertainty and Statistics

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Abstract

Statistics will provide the answer to our fear over the increasing uncertainty in chip performance. Our “confidence” in the correct operation of our integrated circuits will take on a new probabilistic meaning. This presentation will make the case for statistical optimization of integrated circuits in order to ensure high performance, yield and robustness. Today’s discrete and continuous optimization techniques are not up to the task. New metrics will be required to allow physical synthesis tools to target these new optimization criteria. This presentation will describe the form that such metrics will take, and predict a phased introduction of statistical criteria in the optimization and automated fix-up process.

Categories & Subject Descriptors: B.7.2 [Design Aids]: Simulation; B.8.2 [Performance and Reliability]: Performance Analysis and Design Aids

General Terms: Algorithms, Performance, Design, Reliability, Verification.

Keywords: Statistical timing, statistical optimization.

Bio

Chandu Visweswariah received a Ph.D. in Computer Engineering from Carnegie Mellon University in 1989 and has been a Research Staff Member at the IBM Thomas J. Watson Research Center since. He presently manages a circuit and interconnect analysis group. He has developed circuit simulation, circuit optimization and statistical timing tools. He is the author or co-author of one book and over 50 publications; he holds 12 U.S. patents with 15 more in the pipeline. In 2002, he was a visiting faculty at the Eindhoven University of Technology. In 2003 he won an IBM Corporate award for his work on formal circuit optimization. He won a Best Paper award at DAC 2004 and his team won the EDN “Innovation of the Year (EDA Tools Category)” and “Innovator of the Year” awards in 2006. Chandu is a Fellow of the IEEE.