Statistical Analysis and Optimization in the Presence of Gate and Interconnect Delay Variations

[Extended Abstract]

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1. ABSTRACT

Increasing variability in gate and wire delays of integrated circuits makes timing verification and optimization very challenging tasks [3]. Variability can be because of manufacturing processes, environmental sources (e.g., temperature or V_{dd}) or fatigue effects (NBTI and hot electrons). Due to processing steps like CMP (Chemical Mechanical Polishing) or RIE (Reactive Ion Etching), on-chip interconnects have variable width, height and inter-layer dielectric thicknesses.

With each generation of technology, the number and proportional impact of these variations is increasing. Worst-casing all sources of variation is not feasible, and statistical timing [4, 1] has proven to be an effective way to deal with this variability. The main advantages of statistical timing are the ability to reduce pessimism compared to exhaustive corner-based timing, and efficient coverage of the entire process space. So-called block-based statistical timing methods [4] are incremental and therefore can be used in the inner loop of an optimization or physical synthesis flow.

This invited presentation will describe how interconnect variations are modeled for statistical timing purposes. The extraction and variational modeling of gate and interconnect delay will be described [7]. Thicker wires are less resistive and reduce interconnect delay at the expense of higher gate delay due to increased capacitance. Thinner wires, on the other hand, increase net delay but provide more resistive shielding.

In a statistical timing framework, the critical path is not unique. In fact, each point in the process space can have a different critical path. In such a scenario, traditional "deterministic" timing margin or slack is not a good metric for improving the timing performance of a design across the entire process space. A new metric called criticality probability [4, 5, 6] is proposed for simultaneous optimization across the entire process space [2].

In summary, a variational delay modeling methodology combined with incremental statistical timing allows for the systematic analysis of circuit performance in the presence of variability. In addition, diagnostics such as process sensitivities and criticality probabilities will enable the optimization of circuits across the entire process space.

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3. REFERENCES

[1] H. Chang and S. S. Sapatnekar. Statistical timing analysis considering spatial correlations using a single PERT-like traversal. *IEEE International Conference on Computer-Aided Design*, pages 621–625, November 2003. San Jose, CA.

[2] M. R. Guthaus, N. Venkateswaran, C. Visweswariah, and V. Zolotov. Gate sizing using incremental parameterized statistical timing analysis. *IEEE International Conference on Computer-Aided Design*, pages 1029–1036, November 2005. San Jose, CA.

[3] C. Visweswariah. Death, taxes and failing chips. *Proc. 2003 Design Automation Conference*, pages 343–347, June 2003. Anaheim, CA.

[4] C. Visweswariah, K. Ravindran, K. Kalafala, S. G. Walker, and S. Narayan. First-order incremental block-based statistical timing analysis. *Proc. 2004 Design Automation Conference*, pages 331–336, June 2004. San Diego, CA.

[5] J. Xiong, V. Zolotov, C. Visweswariah, and N. Venkateswaran. Criticality computation in parameterized statistical timing. *Proc. 2006 TAU (ACM/IEEE workshop on timing issues in the specification and synthesis of digital systems)*, February 2006. San Jose, CA, submitted for review.

[6] J. Xiong, V. Zolotov, C. Visweswariah, and N. Venkateswaran. Criticality computation in parameterized statistical timing. *Proc. 2006 Design Automation Conference*, July 2006. San Francisco, CA, submitted for review.

[7] P. S. Zuchowski, P. A. Habitz, J. D. Hayes, and J. H. Oppold. Process and environmental variation impacts on asic timing. *IEEE International Conference on Computer-Aided Design*, pages 336–342, November 2004. San Jose, CA.

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