

# Formal Static Optimization of High-Performance Digital Circuits

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## ABSTRACT

Static circuit optimization implies sizing of transistors and wires on a static timing basis, taking into account all paths through a circuit. This invited presentation will describe static circuit optimization using formal nonlinear optimization with the guarantee of convergence to a local minimum. The optimization is based on transistor-level static timing analysis, and fast time-domain simulation and gradient computation methods. Static circuit optimization leads to higher quality designs, enables designers to easily compare alternative topologies and better understand the tradeoffs involved. Several high-performance microprocessor macros have benefited from this type of optimization.

## 1. SUMMARY AND OUTLINE

This presentation will describe EinsTuner, a state-of-the-art, formal, transistor-level, static circuit optimizer, including the algorithms involved, the software components, and the methodology and benefits of using the tool.

Given a timing graph, EinsTuner employs a unique formulation of the static optimization problem [1]. Unfortunately, the straightforward formulation leads to problems that are very large, degenerate and redundant. Arrival time pruning [2] addresses these problems and leads to more compact and numerically better conditioned optimization problems.

Circuit optimization problems are typically stated as a minimization of the cycle time subject to area, input loading, internal slew (rise/fall time), output slew and  $\beta$  ratio constraints.

The timing graph and the necessary simulation information to determine the delay and slew of each arc in the timing graph are obtained from a transistor-level static timing analyzer called EinsTLT [3]. Arbitrary transistor topologies are accommodated.

During the optimization, the delays and slews of each arc in the timing graph must be computed efficiently. EinsTuner uses SPECS [4], a fast, event-driven timing simulator with simplified device models. In addition, the sensitivity (gradi-

ent) of each delay and slew with respect to transistor widths, fanout capacitances and input slews are computed by the adjoint method [5]. The sensitivity computation is an indispensable part of gradient-based solution of large, nonlinear optimization problems.

The optimization problem at hand can often contain as many as 50,000 constraints and 50,000 variables. The solution of these problems is obtained using LANCELOT [6], a large-scale, general-purpose nonlinear optimization package. LANCELOT has been heavily tailored for the circuit optimization problem, including choices of optimization criteria, initializations and two-step updating [7]. If time permits, results from experiments with Lagrangian Relaxation algorithms [8] will be presented.

Application of EinsTuner leads to 10% or more improvement on even previously hand-tuned circuits. The gains are more impressive on synthesized circuits and untuned circuits. Further, designers' productivity in exploring tradeoffs and alternative topologies is enhanced. Results of using EinsTuner and the corresponding methodology impact will be discussed.

## 2. REFERENCES

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