

# Chandu Visweswariah

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## Work

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## EDUCATION

**Carnegie Mellon University** (7/1987 - 5/1989) Pittsburgh, PA  
**Doctor of Philosophy** in Electrical and Computer Engineering. (Cumulative GPA: 4.00). Ph.D. supported by AT&T Bell Laboratories, Murray Hill, NJ. Advisor: Prof. Ronald A. Rohrer.

**Doctoral thesis:** "Piecewise approximate circuit simulation." This thesis proposes a new tree/link-based simulation methodology that allows for piecewise approximate, event-driven, mixed-accuracy simulation using table models for device evaluation. A prototype simulator was created which yielded speedups over conventional simulation techniques on a number of large industrial circuits from Harris Semiconductor, Texas Instruments and Intel Corp.

**Carnegie Mellon University** (8/1985 - 10/1986) Pittsburgh, PA.  
**Master of Science** in Electrical and Computer Engineering. (Cumulative GPA: 4.00). Advisor: Prof. Ronald A. Rohrer

**Master's thesis:** "SPECS2: a timing simulator." This thesis described some of the ideas that formed the basis of mixed accuracy simulation investigated during the course of the Ph.D. Emphasis was placed on mixed accuracy simulation and the formulation of an oscillation prevention algorithm.

**Indian Institute of Technology** (7/1980 - 6/1985) Chennai (formerly Madras), India  
**Bachelor of Technology** in Electrical Engineering (Electronics). (Cumulative GPA: 3.79). Advisors: Profs. H. N. Mahabala and K. N. Bhat.

**Bachelor's thesis:** "WARMOSS: a time-domain integrated circuit simulator based on waveform relaxation." This thesis described the simulation of MOSFET and GaAs MESFET circuits using waveform relaxation.

## RESEARCH INTERESTS

Circuit simulation, device modeling, circuit optimization, static timing, statistical timing analysis, nonlinear optimization, gradient computation, adjoint methods, VLSI design, timing simulation, design for manufacturability (DFM) and design for profit (DFP), mixed-mode simulation, CAD tools and novel devices.

## INDUSTRIAL EXPERIENCE

**IBM T. J. Watson Research Center** (*9/1989 - present*) Yorktown Heights, NY

**Manager, circuit and interconnect analysis:** (*5/2004 - present*) Line management of a group of researchers working on various aspects of circuit and interconnect analysis, including such duties as recruiting, personnel evaluations, individual development, funding, planning and coordination of projects. Projects managed include the following.

- Maise state-of-the-art reduced order modeling and analysis package for linear interconnects, including sensitivity analysis.
- Nova full-chip and package power delivery analysis, power integrity analysis and decoupling capacitance optimization system.
- IBMcio 3-dimensional time- and frequency-domain mixed electromagnetic and circuit solver.
- EinsStat statistical timing analysis tool (see below for more details).
- ASST for at-speed structural testing of ASIC chips (see below for more details).
- Current source modeling for improved modeling of gates for timing, power and noise.
- Statistical power modeling in order to correlate power with timing in the face of process variations.
- A project aimed at capacitance and impedance extraction of lines with rough surfaces.
- An IBM “Engineering and Technology Services (E&TS)” consulting project with AMD on power and signal integrity with power distribution by means of on-chip planes.
- A power delivery analysis convergence (PDAC) project to converge and consolidate the various power delivery analysis efforts within the company.

**Research Staff Member:** Worked on the research and development of various computer-aided design (CAD) tools for VLSI design (*9/1989 - present*).

EinsStat (2002-present): EinsStat is a statistical timing analysis program in the EinsTimer framework. This project was started in summer 2002, motivated by increasing parametric variability in digital circuit behavior due to manufacturing, environmental and aging variations. Proposed the project, lobbied for a development team to be formed, helped with planning and coordination of the project, and developed and deployed two core statistical timing engines. The first is block-based EinsStat, a linear-time statistical timer that takes both correlated randomness and independent randomness into account. The timer is fully incremental, making it amenable to use by physical synthesis. Sensitivities are stored in a sparse format to enable a large number of sources of variation. The software supports all the usual timer features such as early- and late-mode timing, multiple phases, same- and opposite-mode tests, clock overrides, priority groups, transparent latches with loop-cut tests, statistical CPPR (Common Path Pessimism Removal) support, statistical guard times, and various kinds of reports. All types of sequential circuits and their concomitant timing tests are supported. Multi-million-gate ASIC chips are analyzed in reasonable CPU time. Also developed algorithms for efficiently computing

diagnostics such as criticality probabilities, which are useful during optimization. **EinsStat** supports non-Gaussian and nonlinear sources of variation. Developed a preliminary transistor-level version of **block-based EinsStat**. **EinsStat** also has support for arbitrary spatial correlations. **EinsStat** includes support for statistical slew propagation and a general-purpose Monte Carlo engine called **EinsMC**.

**Block-based EinsStat** has had a profound impact on IBM's products.

- **EinsStat** is a required timing sign-off tool for all 65 nm ASIC chips as of March 2007. It also serves as the timer that guides optimization.
- Over \$24M of intellectual property revenue has been obtained by licensing **EinsStat** software and patents.
- A transistor-level version of **EinsStat** including timing and abstraction methodologies is being developed for server microprocessor designs.
- **EinsStat** is integrated with the *RAPIDS* physical synthesis tool for optimization and fix-up.
- **EinsStat** provides *RSS* credit due to independent randomness in the inner loop of variation-aware timing (**EinsVAT**).
- **EinsStat** was used for transistor-level timing of SRAM macros in custom processors.
- **EinsStat** was a Research Division Accomplishment in 2006 and upgraded to an Outstanding Accomplishment in 2007.

The second timing engine is **path-based EinsStat** which conducts a detailed statistical timing analysis of a set of nominally critical paths in a digital circuit. Implemented four different statistical timing algorithms in this context (the parallelepiped method, the ellipsoid method, the binding probability method and a Monte Carlo method). These methods complement each other to cover both high- and low-dimensionality situations and both high- and low-accuracy requirements. Implemented a path filtering capability in **path-based EinsStat**. Deployed **path-based EinsStat** for back-end-of-the-line (BEOL) probability-of-failure analysis of ASIC chips in November 2003.

ASST (2006-present): At-Speed Structural Test (**ASST**) is used to test IBM's 65 nm ASIC chips. Criticality analysis in **EinsStat** is leveraged to choose critical paths for sensitization during at-speed test in order to obtain the best possible process coverage. This novel test methodology was developed to maintain high quality of shipped chips even in the face of large process variations.

Deft (2003-present): **Deft** (**DE**rivative **F**ree **T**uner) is a circuit optimizer for small circuits that require the accuracy and generality of SPICE simulation. It uses the DFO optimization package developed by K. Scheinberg *et al* at the IBM T. J. Watson Research Center, and efficient repeated circuit simulation runs with PowerSpice's GODATA capability. **Deft** supports arbitrary simple bounds, linear and nonlinear constraints, equality and inequality constraints and minimax problems. A novel failure recovery scheme is implemented in **Deft**. A family of "measurement widgets" that automatically detect electrical failure is provided with the tool. **Deft** has been used for numerous circuit tuning tasks in various contexts. Most notable, perhaps, are its use in tuning individual ASIC library cells and in tuning clock-distribution circuits for high-performance microprocessors.

EinsTuner (1997-present): EinsTuner is a circuit optimization tool based on static timing analysis. EinsTuner's formulation of the optimization problem is unique and it utilizes state-of-the-art nonlinear optimization methods and adjoint gradient computation techniques to solve the tuning problem. Custom circuits are accommodated by means of dynamic simulation and gradient computation on the fly. A wide variety of digital circuits are handled including combinational circuits, master/slave latches, transparent latches, multi-cycle paths, multi-frequency circuits, clock blocks, interconnect models, etc. A wide variety of constraints such as area, delay, input loading,  $\beta$  ratio, ratio-ing and slew limits are supported. The tuning has also been applied to synthesized Random Logic Macros (RLMs) by means of a methodology called "partial RLM tuning," in which an *in situ* marking of timing critical logic is employed to tune large macros. Various modes of tuning such as delay minimization, area minimization, FAR (Free Area Recovery), TPS (Total Positive Slack) and tradeoff mode have been implemented. A parallel version of EinsTuner was released in mid-2003, yielding a speedup of between 2.5x and 3x on a 4-processor machine.

Proposed the project, and developed a prototype implementation. Developed several innovations to render the optimization feasible, efficient and effective. Among them is a unique graph-based pruning algorithm that reduces the size of the optimization problem while reducing redundancy and degeneracy. Another innovation is exploitation of optimality conditions to improve robustness and numerical convergence. Another idea is an "uncertainty-aware" tuning mode. In 2000 and 2001, was the team leader of a Fishkill-based team to develop a corporate-wide production version of EinsTuner. Deployed the tool to various microprocessor development groups, including planning enhancements, developing and testing the tool, and managing customer relations.

EinsTuner has been applied to custom, semi-custom and synthesized logic. Both flat and hierarchical, and both schematic and extracted netlists are accommodated. Significant benefits from EinsTuner were realized by S/390 microprocessor chips (Alliance '98, Alliance '00 "Freeway," Alliance '03 "Bluefire," TSaurus, eCLipz), the PowerPC chips GP/Spinnaker, GPuL, GQ and GR, and the Sony-Toshiba-IBM game processor ("Cell").

JiffyTune (1995-1998): Conducted research in the area of circuit optimization and developed JiffyTune, a dynamic circuit tuning tool. JiffyTune automatically adjusts the sizes of wires and transistors in a schematic to meet delay, area, power, noise, manufacturability and rise/fall time targets. It optimizes custom, high-performance circuits. It uses SPECS, a fast simulator with transient sensitivity computation in the inner optimization loop and LANCELOT, a state-of-the-art nonlinear optimization package. Was the main developer of the JiffyTune engine, including the use of adjoint methods for sensitivity computation and application of nonlinear optimization. JiffyTune has been used by several chip designs in IBM including PowerPC 630fp, PowerPC 630fp+, Harp macro for a disk drive controller, S/390 microprocessors and the Logical Panel Module chip. Several innovations such as tuning for manufacturability and accommodation of noise considerations during optimization were implemented in JiffyTune.

Mixed-mode simulation (1993-1995): Developed and investigated a mixed-mode simulation (or co-simulation) system by means of a simulation backplane, including the following activities:

- Participated in the CFI (CAD Framework Initiative) committee to set standards for co-simulation and simulation backplanes (1992-1993).

- Conducted an IBM internal survey and study on the need for mixed-mode simulation within IBM and made recommendations.
- Developed a prototype along with tools from Viewlogic and Precedence Inc. (both of Santa Clara, CA) that was demonstrated at the Design Automation Conference, Dallas, TX, in June 1993 and the Design Automation Conference, San Diego, CA, in June 1994. The demonstration involved co-simulation between SPECS (IBM circuit simulator), AUSSIM (IBM gate-level logic simulator) and ViewSim (Viewlogic gate-level logic simulator) via the Precedence backplane.
- Represented IBM Research at the “Mixed Analog/Digital Subgroup” of the IBM Low-end Methodology Committee.

**SPECS (1989-present):** (**S**imulation **P**rogram for **E**lectronic **C**ircuits and **S**ystems) Conducted research in the area of new algorithms for the approximate time-domain simulation of very large scale integrated circuits. These algorithms use piecewise approximations of nonlinear device characteristics. Simulation is event-driven and runs two orders of magnitude faster than IBM’s SPICE-like simulator, AS/X. Worked on all aspects of the project over the course of numerous software releases including algorithms, software architecture, development, device modeling, power estimation, project planning, presentations to and interactions with designers, support, testing, MOTIF interfaces, interactive simulation modes and documentation. SPECS was used in production at 11 different sites of IBM on various chips including several SRAM, DRAM and microprocessor designs such as Grizzly (1M CMOS5L SRAM), Kodiak (1M CMOS5S SRAM), PowerPC 601 SRAM macro, Chancellor/Equity/LIBC SRAM macro, Luna-C 16 Mb DRAM, Shrink2 4 Mb DRAM, 486 SLC/2 (Bimini 2-SX/LP) clock shaper, “Blue Lightning” clock-tripled 486 chip, MONET-J, Lindau PLL, high-speed read channel for magnetic recording, Harp macro, Logical Panel Module chip, Alliance S/390 microprocessor and several cache and ABIST circuits. SPECS is presently used in EinsTuner as the simulator that computes delays and gradients of individual gates. Various aspects of SPECS such as efficient sensitivity computation, chain-ruling of modeling equations, efficient simulation of interconnect and dynamic adaptive model resolution continue to be active topics of investigation.

**Harris Semiconductor** (8/1988) Melbourne, FL  
**Consultant:** Transferred simulation technology; benchmarked simulator on industrial circuits; developed device models; formulated designer guidelines.

**AT&T Bell Laboratories** (11/1986 - 5/1987) Murray Hill, NJ  
**Research Intern:** Assisted in developing a high-level analog macromodeling methodology. Developed ACME (**A**nalog **C** **M**odel **E**valuator), a tool to verify and debug individual analog macromodels. Developed tools called MODGENS and MODGENZ to automatically generate analog macromodels for subcircuits described as transfer functions in the Laplace- and z-domains, respectively. Assisted in the incorporation of analog macromodels in the mixed mode simulator, MOTIS3.

**Texas Instruments** (10/1988) Dallas, TX  
**Visiting Engineer:** Installed SPECS and simulated benchmark circuits.

**Tata Institute of Fundamental Research** (5/1984 - 7/1984) Mumbai, India  
**Research Assistant:** Investigated nonlinear transient simulation of integrated circuits by the waveform relaxation method; implemented a prototype software package.

**ACADEMIC  
EXPERIENCE**

**Eindhoven Univ. of Technology** (4/2002 - 8/2002) Eindhoven, The Netherlands  
**Visiting Assistant Professor:** Sabbatical assignment in the Electrical Engineering department. Taught a senior-level undergraduate class “5L050 Ontwerptechnologie” (Design Technology) on the basics of CAD algorithms, including simulation, modeling, static timing and sensitivity analysis. Advised graduate students in Prof. R. H. J. M. Otten’s group.

**University of Coimbra** (10/16/1997 - 10/29/1997) Coimbra, Portugal  
**Visiting researcher:** Conducted research in “Two-step Updating” algorithms in the context of nonlinear optimization at the Department of Mathematics.

**IBM T. J. Watson Research Center** (9/1992 - 12/1992) Yorktown Heights, NY  
Taught a 10-part course on circuit simulation fundamentals to IBM engineers, which was well received and attended. The course materials formed the basis of a subsequent text book on circuit simulation published by McGraw Hill in 1995.

**Carnegie Mellon University** (6/1989 - 8/1989) Pittsburgh, PA  
**Visiting Research Associate:** Prepared and conducted a technology transfer course (TTC) on SPECS organized by the Semiconductor Research Corporation (SRC) and attended by fifteen delegates from various microelectronics companies.

**Carnegie-Mellon University** (8/1985 - 10/1986 & 7/1987 - 5/1989) Pittsburgh, PA  
**Research Assistant in the CAD Group:** Built an 8-bit microprocessor based on the Am 2903 and 2910 bit-slice chips. Implemented a placement and routing package for gate arrays and a program to automatically generate stack layouts. Designed a data path layout. As part of a group project, wrote a circuit simulator to analyze circuits based on the tree/link formulation of equations and an explicit solution method.

**Carnegie Mellon University** (7/1987 - 8/1989) Pittsburgh, PA  
Wrote a grant proposal which was accepted by the NSF to fund the group’s graduate research.

**Carnegie Mellon University** (8/1988 - 12/1988) Pittsburgh, PA  
**Teaching Intern:** Assisted in teaching the graduate level course, “Circuit Theory.”

**Network for Education, Services and Training** (1983 - 1985) Chennai, India  
**Voluntary Teaching Program Co-ordinator:** Co-ordinated a project aimed at coaching underprivileged students towards engineering university entrance examinations.

**Indian Institute of Technology** (6/1984 - 6/1985) Chennai, India  
**Teaching Assistant:** Assisted in teaching the courses “Introduction to Computing” and “Computer Organization.”

**GRANTED  
PATENTS**

1. N. Venkateswaran, C. Visweswariah, J. Xiong, and V. Zolotov. *System and method of criticality prediction in statistical timing analysis*. U.S. patent 7,437,697, issued October 2008.
2. C. Visweswariah. *System and method for statistical timing analysis of digital circuits*. U.S. patent 7,428,716, issued September 2008.

3. C. Visweswariah. *System and method for statistical timing analysis of digital circuits*. China patent ZL200410078630.7, issued November 2007.
4. C. Visweswariah. *System and method for statistical timing analysis of digital circuits*. Japan patent 4,061,295, issued December 2007.
5. K. Kalafala, V. B. Rao, and C. Visweswariah. *Affinity-based clustering of vectors for partitioning the columns of a matrix*. U.S. Patent 7,353,359, issued April 2008.
6. H. Chang, S. Narayan, C. Visweswariah, and V. Zolotov. *System and method for accommodating non-Gaussian and nonlinear sources of variation in statistical static timing analysis*. U.S. Patent 7,293,248, issued November 2007.
7. N. Venkateswaran, C. Visweswariah, L. Zhang, and V. Zolotov. *Method, system and program product for accommodating a spatially correlated source of variation in statistical timing analysis*. U.S. Patent 7,212,946, issued May 2007.
8. K. Kalafala, P. Qi, A. J. Suess, D. J. Hathaway, and C. Visweswariah. *System and method for correlated process pessimism removal for static timing analysis*. U.S. Patent 7,117,466, issued October 2006.
9. S. G. Walker, C. Visweswariah, K. Scheinberg, and P. J. Restle. *System and method for derivative-free optimization of electrical circuits*. U.S. Patent 7,117,455, issued October 2006.
10. C. Visweswariah. *System and method for incremental statistical timing analysis of digital circuits*. U.S. Patent 7,111,260, issued September 2006.
11. E. K. Cho, D. J. Hathaway, M-T. Hsu, L. K. Lange, G. A. Northrop, C. Visweswariah, C. Washburn, P. M. Williams, and J. Zhou. *A methodology for tuning synthesized random logic macro circuits in a continuous design space with optional insertion of multiple threshold voltage devices*. U.S. Patent 7,093,208, issued August 2006.
12. C. Visweswariah. *System and method for probabilistic criticality prediction of digital circuits*. U.S. Patent 7,086,023, issued August 2006.
13. D. J. Hathaway, L. K. Lange, C. Visweswariah, and P. M. Williams. *Method of optimizing and analyzing selected portions of a digital integrated circuit*. U.S. Patent 7,010,763, issued March 2006.
14. D. J. Hathaway, C. Visweswariah, P. M. Williams, and J. Zhou. *Method of achieving timing closure in digital integrated circuits by optimizing individual macros*. U.S. Patent 7,003,747, issued February 2006.
15. C. Visweswariah. *System and method for optimal waveform shaping*. U.S. patent 6,922,819 issued July 2005.
16. X. Bai, D. J. Hathaway, P. N. Strenski, and C. Visweswariah. *Parameter variation tolerant method for circuit design optimization*. U.S. patent 6,826,733, issued November 2004.
17. A. R. Conn and C. Visweswariah. *Method of reformulating static circuit optimization problems for reduced size, degeneracy and redundancy*. U.S. patent 6,321,362, issued November 2001.

18. A. R. Conn, R. A. Haring, and C. Visweswariah. *Method for incorporating noise considerations in automatic circuit optimization*. U.S. patent 5,999,714, issued December 1999.
19. A. R. Conn, R. A. Haring, and C. Visweswariah. *Method of efficient gradient computation*. U.S. patent 5,886,908, issued March 1999.

**PENDING  
PATENTS**

1. S. Abbaspour, P. Feldmann, D. D. Ling, and C. Visweswariah. *System and method for converting an arbitrary waveform into an effective ramp for timing analysis*. Docket YOR-8-2008-????, to be filed.
2. C. Visweswariah, J. Xiong, and V. Zolotov. *System and method for variation-aware test pattern generation*. Docket YOR-8-2008-1136, to be filed.
3. J. G. Hemmett and C. Visweswariah. *A method for improved Monte Carlo based statistical maximum and minimum operations*. Docket BUR-9-2008-0376-US1, to be filed.
4. N. Buck, H. Chen, J. Eckhardt, E. A. Foreman, J. Gregerson, P. A. Habitz, S. Lichtensteiger, and T. Wilder. *Methodology to optimize chips for profit weighted performance process and environment variation*. Docket BUR-9-2008-0370-US1, to be filed.
5. E. A. Foreman, P. A. Habitz, D. Sinha, N. Venkateswaran, C. Visweswariah, and V. Zolotov. *Methods for mixed mode statistical and deterministic timing analysis*. Docket FIS-9-2008-0368-US1, to be filed.
6. A. Bhanji, B. Dorfman, K. Kalafala, D. Sinha, N. Venkateswaran, and C. Visweswariah. *A method of statistical timing abstraction of VLSI circuits*. Docket FIS-9-2008-0342-US1, to be filed.
7. Y. Shi, C. Visweswariah, J. Xiong, and V. Zolotov. *System and method for multi-layer process space coverage and path selection for at-speed testing*. Docket YOR-9-2008-0547-US1, to be filed.
8. D. Sinha, N. Venkateswaran, C. Visweswariah, J. Xiong, and V. Zolotov. *Reversible statistical maximum and minimum operations for efficient incremental statistical timing analysis and optimization*. Docket YOR-9-2008-0317-US1, to be filed.
9. N. Buck, B. M. Dreibelbis, J. Dubuque, E. A. Foreman, P. A. Habitz, G. M. Schaeffer, and C. Visweswariah. *Method and system for analyzing cross-talk coupling noise events in block-based statistical static timing*. Docket BUR-9-2008-0192-US1, filed June 2008.
10. J. G. Hemmett, C. Visweswariah, and V. Zolotov. *Methods for statistical slew propagation during block-based statistical static timing*. Docket BUR-9-2008-0093, filed May 2008.
11. N. Buck, J. Dubuque, E. A. Foreman, P. A. Habitz, and C. Visweswariah. *Method for identifying failing timing requirement in a digital design*. Docket BUR-9-2008-0057-US1, filed April 2008.

12. H. Fatemi, C. Visweswariah, J. Xiong, and V. Zolotov. *Method and apparatus for statistical path selection for at-speed testing*. Docket YOR-9-2007-0613-US1, filed April 2008.
13. J. G. Hemmett, N. Venkateswaran, C. Visweswariah, and V. Zolotov. *Methods for conserving memory in statistical static timing analysis*. Docket BUR-9-2008-0017-US1, filed March 2008.
14. N. Buck, J. Dubuque, E. A. Foreman, P. A. Habitz, and C. Visweswariah. *Method to identify timing violations outside of manufacturing spec limits*. Docket BUR-9-2007-0265-US1, filed March 2008.
15. N. Buck, J. Dubuque, E. A. Foreman, P. A. Habitz, K. Kalafala, G. M. Schaeffer, and C. Visweswariah. *Timing closure using multiple timing runs which distribute the frequency of identified fails per timing corner*. Docket BUR-9-2007-0264-US1, filed February 2008.
16. L. S. Chadwick, J. A. Culp, D. J. Hathaway, T. Hook, K. Peterson, A. Polson, C. Visweswariah, and O. Takahashi. *Compensating for area of unmatched perimeter density*. Docket BUR-9-2007-0267-US1, filed February 2008.
17. C. Visweswariah, J. Xiong, and V. Zolotov. *Method and apparatus for computing test margins for at-speed testing*. Docket YOR-9-2007-0614-US1, filed January 2008.
18. V. Iyengar, D. Lackey, S. Venkatesan, C. Visweswariah, and J. Xiong. *Critical path selection for at-speed test*. Docket BUR-9-2007-0146-US1, filed December 2007.
19. G. Grise, P. A. Habitz, V. Iyengar, D. Lackey, C. Visweswariah, and V. Zolotov. *System and method for generating at-speed structural tests to improve process and environmental parameter space coverage*. Docket BUR-9-2006-0231-US1, filed November 2007.
20. C. Visweswariah, J. Xiong, and V. Zolotov. *Method and apparatus for incrementally computing criticality and yield gradient*. Docket YOR-9-2007-0374-US1, filed October 2007.
21. D. Lackey, C. Visweswariah, and P. Zuchowski. *Method and device for selectively adding timing margin in an integrated circuit*. Docket BUR-9-2007-0075-US1, filed October 2007.
22. S. Abbaspour, D. J. Hathaway, C. Visweswariah, J. Xiong, and V. Zolotov. *Representing and propagating a variational voltage waveform in statistical static timing analysis of digital circuits*. Docket YOR-9-2006-0597-US1, filed April 2007.
23. E. A. Foreman, G. Grise, P. A. Habitz, V. Iyengar, D. Lackey, C. Visweswariah, and V. Zolotov. *IC chip at-functional-speed testing with process coverage evaluation*. Docket BUR-9-2006-0235-US1, filed April 2007.
24. N. Buck, J. Dubuque, E. A. Foreman, P. A. Habitz, K. Kalafala, P. Qi, C. Visweswariah, and X. Wang. *Parameter ordering for multi-corner static timing analysis*. Docket BUR-9-2007-0038-US1, filed February 2007.
25. N. Buck, J. Dubuque, E. A. Foreman, P. A. Habitz, K. Kalafala, P. Qi, C. Visweswariah, and X. Wang. *Variable threshold system and method for multi-corner static timing analysis*. Docket BUR-9-2006-0219-US1, filed February 2007.

26. N. Buck, J. Dubuque, E. A. Foreman, P. A. Habitz, K. Kalafala, P. Qi, C. Visweswariah, and X. Wang. *Method and system of evaluating statistical sensitivity credit in path-based hybrid multi-corner static timing analysis*. Docket BUR-9-2006-0236-US1, filed February 2007.
27. S. Abbaspour, G. M. Schaeffer, and C. Visweswariah. *Method and apparatus for static timing analysis in the presence of a coupling event and process variation*. Docket YOR-9-2006-0628-US1, filed January 2007.
28. R. Banerji, D. J. Hathaway, K. Kalafala, J. M. Sheridan, and C. Visweswariah. *System and method for efficient analysis of point-to-point delay constraints in static timing*. Docket FIS-9-2006-0335-US1, filed December 2006.
29. C. Visweswariah, J. Xiong, and V. Zolotov. *Method, system and program product for computing a yield gradient from statistical timing*. Docket YOR-9-2005-0500-US1, filed February 2006.
30. J. A. G. Jess and C. Visweswariah. *System and method for statistical modeling and statistical timing analysis of integrated circuits*. Docket YOR-9-2002-0156-US1, filed June 2002.

## **PUBLICATIONS**   **Book**

- [1] L. T. Pillage, R. A. Rohrer, and C. Visweswariah. *Electronic circuit and system simulation methods*. McGraw-Hill, 1995.

### **Book chapter**

- [1] C. Visweswariah. Electrical and timing simulation. In J. G. Webster, editor, *Encyclopedia of Electrical and Electronics Engineering*, volume 6, pages 229–238. John Wiley and Sons, 1999.

### **Invited publications**

- [1] C. Visweswariah. Robustness and quality in the face of variability. *IEEE International Symposium on Quality Electronic Design*, March 2008. Keynote speech, San Jose, CA.
- [2] C. Visweswariah. Within-die variations in timing: from derating to CPPR to statistical methods. *IEEE International Conference on Computer-Aided Design*, November 2007. Full-day tutorial, San Jose, CA.
- [3] C. Visweswariah. Statistical techniques to combat variability and achieve robust design. *Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI)*, October 2007. Invite talk, Sapporo, Japan.
- [4] C. Visweswariah. The end of traditional cmos. *Workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI)*, October 2007. Panel opening statement, Sapporo, Japan.
- [5] C. Visweswariah. Statistical techniques for robust digital design. *University of Texas Seminar Series*, March 2007. Austin, TX.

- [6] C. Visweswariah. Fear, uncertainty and statistics. *Proc. International Symposium on Physical Design (ISPD)*, March 2007. Invited talk, Austin, TX.
- [7] C. Visweswariah. What engineers want. *Optimization and Engineering Workshop, Panel opening statement*, November 2006. Banff International Research Station for Mathematical Innovation and Discovery (BIRS), Banff, Alberta, Canada.
- [8] C. Visweswariah. Challenges in statistical timing and optimization of integrated circuits. *Optimization and Engineering Workshop*, November 2006. Banff International Research Station for Mathematical Innovation and Discovery (BIRS), Banff, Alberta, Canada.
- [9] C. Visweswariah. Statistical timing in a practical 65 nm robust design flow. *C2S2 workshop on Robust Circuit Design*, July 2006. Berkeley, CA.
- [10] C. Visweswariah. Statistical analysis and optimization in the presence of gate and interconnect delay variations. *Proc. System Level Interconnect Prediction (SLIP)*, page 37, March 2006. Munich, Germany.
- [11] C. Visweswariah. Can innovation be nurtured? *EE Times*, December 2005. Invited article for special issue on the subject of innovation.
- [12] C. Visweswariah. Statistical analysis and design of digital integrated circuits. *EDA Forum*, November 2005. Invited presentation, Hanover, Germany.
- [13] C. Visweswariah. Mathematics and engineering: a clash of cultures? *Industrial optimization seminar series, The Fields Institute for Research in Mathematical Sciences*, May 2005. Invited presentation, Toronto, Canada.
- [14] C. Visweswariah. Spread sheet studies on the impact of variability. *International Conference on Integrated Circuit Design and Technology (ICICDT)*, May 2005. Invited presentation, Austin, TX.
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## PROFESSIONAL HONORS

IBM Twelfth Plateau Invention Achievement Award, October 2008.

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IBM Tenth Plateau Invention Achievement Award, May 2008.

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IBM Outstanding Research Division Accomplishment for the EInsStat project, January 2008.

IBM Supplemental Patent Issue Award for U.S. Patent 7,117,466 (“System and method for correlated process pessimism removal for static timing analysis”) awarded to “inventors of the top 10% of IBM United States patents that issued during the 2006 calendar year,” December 2007.

IBM Supplemental Patent Issue Award for U.S. Patent 7,093,208 (“Method for tuning a digital design for synthesized random logic circuit macros in a continuous design space with optional insertion of multiple threshold voltage devices”) awarded to “inventors of the top 10% of IBM United States patents that issued during the 2006 calendar year,” May 2007.

IBM Eighth Plateau Invention Achievement Award, December 2007.

IBM Outstanding Innovation Award for “EInsStat (Statistical Timing Tool) IP Revenue,” July 2007.

IBM Seventh Plateau Invention Achievement Award, May 2007.

IBM Sixth Plateau Invention Achievement Award, March 2007.

EDN (Electronic Design News) Innovator of the Year Award, awarded to EInsTimer Statistical Timing (IBM Research), April 2006.

IBM Research Division Accomplishment for the EInsStat project, January 2007.

EDN (Electronic Design News) Innovation of the Year Award in the EDA (Design and Implementation) category, awarded to EInsTimer Statistical Timing (IBM Research),

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2004 Pat Goldberg Memorial IBM Research Best Paper Award in Computer Science, Electrical Engineering and Mathematics for the paper C. Visweswariah, K. Ravindran, K. Kalafala, S. G. Walker and S. Narayan, “First-order incremental block-based statistical timing analysis,” *Design Automation Conference (DAC)*, San Diego, CA, pages 331–336, June 2004.

Elected Fellow of the Institute of Electrical and Electronics Engineers (IEEE), for “contributions to large-scale integrated circuits,” effective January 2005.

Best paper in the “Back-end design” category, Design Automation Conference (DAC) 2004, San Diego, CA, for the paper C. Visweswariah, K. Ravindran, K. Kalafala, S. G. Walker, and S. Narayan, “First-order incremental block-based statistical timing analysis,” pages 331–336.

2003 Pat Goldberg Memorial IBM Research Best Paper Award in Computer Science, Electrical Engineering and Mathematics for the paper J. A. G. Jess, K. Kalafala, S. R. Naidu, R. H. J. M. Otten, and C. Visweswariah, “Statistical timing for parametric yield prediction of digital integrated circuits,” *Design Automation Conference (DAC)*, Anaheim, CA, pages 932–937, June 2003.

IBM Fourth Plateau Invention Achievement Award, June 2004.

IBM Third Plateau Invention Achievement Award, October 2003.

IBM Corporate Award for “Formal Static Circuit Tuning Tool,” June 2003.

IBM Second Plateau Invention Achievement Award, June 2003.

Selection of two papers for the Best of ICCAD volume of 40 of the best papers published during 20 years of the International Conference on CAD (ICCAD):

- C. Visweswariah and R. A. Rohrer, SPECS2: an integrated circuit timing simulator, ICCAD 1987.
- A. R. Conn, P. K. Coulman, R. A. Haring, G. L. Morrill, and C. Visweswariah, Optimization of custom MOS circuits by transistor sizing, ICCAD 1996.

Second prize, Best course among mandatory courses in 2001/2002, Department of Electrical Engineering, Eindhoven University of Technology, Eindhoven, The Netherlands, for teaching the course “5L050 Ontwerptechnologie” (Design Technology) in summer 2002.

IBM First Plateau Invention Achievement Award, June 2002.

IBM Outstanding Technical Achievement Award for “Invention and development of EinsTuner,” December 2001, and invitation to the Corporate Technical Recognition Event (CTRE), June 2002.

IBM Execute Now award for “Design and implementation of the Freeway (G7) microprocessor,” July 2001.

IBM Research Division Accomplishment for the EinsTuner project, January 2001.

IBM Research Division Award for “Expedited release of production EinsTuner,” September 2000.

Contributions to the INFORMS prize, which was awarded to IBM by the Institute for Operations Research and the Management Sciences, November 1999. The prize was awarded to IBM for its “innovative and effective use of operations research and management science (OR/MS) methodology throughout the corporation.” In winning this prize, IBM highlighted five projects, including circuit tuning in JiffyTune and EinsTuner.

IBM Research Division Award for “Design and realization of the Alliance (G5) microprocessor,” November 1998.

IBM Research Division Award for “Contributions to the design and realization of the Alliance (G4) microprocessor,” November 1997.

IBM First Patent Application Invention Achievement Award, June 1997.

IBM Research Division Accomplishment for the JiffyTune project, January 1997.

IBM Quarterly Highlight project of the Computer-Aided Design and Verification department for the JiffyTune project, fourth quarter, 1996.

IBM Blue Chip Award, May 1996.

Elected Senior Member, IEEE, September 1995.

IBM Research Division Technical Group Award for “Contributions to the Alliance first RIT and stand alone bring-up,” December 1995.

McGraw Hill Book of the Month, April 1995.

IBM Outstanding Technical Achievement Award for “Simulation Program for Electronic Circuits and Systems (SPECS),” May 1994.

Fellowship from AT&T Bell Laboratories for the duration of doctoral studies at Carnegie Mellon University.

Best Paper in Session at the Semiconductor Research Corporation (SRC) Techcon, October 1988, for the paper “Mixed accuracy simulation with SPECS.”

Research Assistantship from Carnegie Mellon University for the duration of Master’s studies in the Department of Electrical and Computer Engineering.

Best Paper and Presentation at the IEEE All-India Students' Symposium on "Recent Trends in CAD," October 1984, for the paper "Simulation of MOS integrated circuits by the waveform relaxation method."

Deutscher Akademischer Austauschdienst (DAAD), West Germany: selected based on academic merit for a student exchange program to West Germany, summer 1983.

Certificate of Academic Distinction, Indian Institute of Technology, Chennai, India, 1980 and 1981.

## PROFESSIONAL ACTIVITIES

**Fellow**, IEEE; member, Circuits and Systems Society.

**Panelist**, Net Seminar moderated by Richard Goering, Senior Editor of *EE Times*, on "The Road to Nanometer CMOS," March 2006. The Net Seminar was part of EE Times' "Great Minds, Great Ideas" project.

**Organizer**, full-day tutorial, "Practical Aspects of Coping with Variability: An Electrical View" at the Design Automation Conference, San Francisco, CA, July 2006. Speakers were Dr. X-W. Lin, Director of R&D, Synopsys, Dr. B. Nikolic, Associate Professor, UC Berkeley, Dr. P. A. Habitz of IBM and Dr. R. Radojcic, Qualcomm.

**Member**, task force on "IBM value-add with silicon modeling and statistical timing," November 2005.

**Member**, Technical Program Committee, PAC<sup>2</sup> conference (Power = Architecture, Circuits and Compilers), IBM Thomas J. Watson Research Center, September 2005.

**Session chair and panel moderator** of a special session entitled, "DFM and variability: theory and practice" at the *Design Automation Conference*, Anaheim, CA, June 2005.

**Member**, PhD committee of Srinath R. Naidu (advisor: Prof. Ralph H. J. M. Otten), Department of Electrical Engineering, Eindhoven University of Technology, The Netherlands, thesis "Tuning for yield: towards predictable deep sub-micron manufacturing," July 2004.

**Focus group discussion leader**, "Statistical static timing analysis and optimization: sizzle or fizzle?," at the ACM/IEEE international workshop on timing issues in the specification and synthesis of digital systems (TAU), Austin, TX, February 2004.

**Panel organizer**, "Libraries: lifejacket or straitjacket?" at the Design Automation Conference (DAC), 2003.

**Session organizer**, "Timing abstraction" and "Circuit effects in static timing," Design Automation Conference (DAC), 2002.

**Member, Technical Program Committee**, Design Automation Conference, 2001, 2002 and 2003. Sub-committee chair for "Timing and Simulation" in 2002 and 2003.

**Session chair and organizer**, "Visualization and animation for VLSI design" and

“Novel devices and yield optimization,” and **organizer**, “Signal integrity: avoidance and test techniques,” Design Automation Conference (DAC), 2001.

**PhD recruiter** for IBM (*1/1992 - 1/1998*) from the ECE department of Carnegie Mellon University; responsibilities included two recruiting trips a year, maintenance of a recruiting database, matching of candidates with job openings and maintenance of University relations; helped recruit a number of PhD-level graduates to various divisions of IBM. Participated in “University Relations Re-engineering” in Fall 1994 by organizing roundtable discussions with faculty members to get feedback on IBM’s University programs.

**Member, Technical Program Committee**, International Conference on Computer-Aided Design (ICCAD), 1998.

**Session chair**, “Topics in circuit simulation,” International Conference on Computer-Aided Design (ICCAD), 1998.

**Member, Technical Program Committee**, International Conference on Computer-Aided Design (ICCAD), 1997.

**Session chair**, “High-level power prediction and reduction” and “Timing analysis” and **co-chair**, “Power estimation and modeling” sessions at the International Conference on Computer-Aided Design (ICCAD), 1997.

**Member, Technical Program Committee**, International Conference on Computer-Aided Design (ICCAD), 1996.

**Session chair**, “Advanced numerical simulation techniques” and “Advances in transmission line analysis” and **co-chair**, “Interconnect Characterization and Analysis” sessions at the International Conference on Computer-Aided Design (ICCAD), 1996.

**Member, Technical Program Committee**, Custom Integrated Circuits Conference (CICC), 1996.

**Session chair**, “Device modeling and analog simulation” at the Custom Integrated Circuits Conference (CICC), 1996.

**Co-chair**, IBM internal “Circuit Tuning Workshop,” May 1995; the workshop was attended by 93 IBMers from 10 different sites.

**Member**, PhD committee of Anirudh Devgan (advisor: Prof. Ronald A. Rohrer), Department of Electrical and Computer Engineering, Carnegie Mellon University, thesis “Adaptively controlled explicit simulation” (*11/1993*).

**Member**, PhD committee of Kimon Michaels (advisor: Prof. Andrzej Strojwas), Department of Electrical and Computer Engineering, Carnegie Mellon University, thesis “Variable accuracy device modeling for event-driven circuit simulation” (*3/1993*).

**Member, Technical Program Committee**, International Conference on Computer Design (ICCD), 1992.

**Session chair**, “Circuit and switch-level simulation” session at the International Conference on Computer Design (ICCD), 1992.

**Member**, CAD Framework Initiative (CFI) committee to set standards for co-simulation and simulation backplanes (1992-1993).

**Reviewer** of papers for the IEEE Transactions on Computer-Aided Design of Circuits and Systems, IEEE Transactions on Circuits and Systems, Design Automation Conference (DAC) and International Symposium on Circuits and Systems (ISCAS).

**CLASSES,  
WORKSHOPS,  
INVITED  
LECTURES  
AND MISC.**

Instituted and organized a weekly seminar series on circuit-related topics in IBM East Fishkill, with six sites of IBM attending remotely (*March 2000 to present*).

Instituted and organized a biweekly circuit and interconnect analysis discussion group in Yorktown (*May 2004 to present*).

“First-order incremental block-based statistical timing analysis,” lecture delivered at the Indian Institute of Science, Bangalore, India, August 2004.

Conducted a science outreach program on the subject of polymer science for 4<sup>th</sup> graders at the “National Academy for Learning” school in Bangalore, India, August 2004.

A. R. Conn and C. Visweswariah, “Small changes, large effects – nonlinear optimization and the design of circuits,” invited plenary lecture given by Dr. Conn at *High-performance Algorithms and Software for Nonlinear Optimization*, Ettore Majorana Center for Scientific Culture, International School of Mathematics, Erice, Italy, July 2001.

A. R. Conn and C. Visweswariah, “Large-scale nonlinear optimization and the design of circuits,” invited plenary lecture given by Dr. Conn at the *International Conference on Optimization and Optimal Control (ICOOC)*, National Cheng Kung University, Tainan, Taiwan, June 2001.

A. R. Conn and C. Visweswariah, “Small changes, large effects – nonlinear optimization and the design of circuits,” invited plenary lecture given by Dr. Conn at the *Seventh US-Mexico Workshop in Numerical Analysis*, Merida, Yucatan, Mexico, January 2001.

Delivered a full-day tutorial at the Design Automation Conference (DAC), 2000 (one of four speakers).

Member, “IBM Futures Team.” Contributed to the development of IBM Research’s “Ten Year Outlook” technology forecasting document, Summer 1998. Focused on the future of biotechnology and nanotechnology.

Invited lecture, “Gradient-based optimization of custom circuits... the second generation,” University of California, Berkeley, November 1998.

Invited lecture, “Gradient-based optimization of custom circuits... the second generation,” IEEE Bangalore Section, India, October 1998.

Delivered a full-day tutorial at the International Conference on Computer-Aided Design (ICCAD), 1996 (one of three speakers).

Invited lecture, “Optimization of custom MOS circuits by transistor sizing,” at Fujitsu Labs. of America, Santa Clara, CA, November 1996.

Member, “Retention Task Force,” IBM T. J. Watson Research Center, 1995.

Speaker at the IBM System, Science and Technology Seminar series, “Breaking the bottleneck,” February 1995.

Classes and workshops attended:

- “Communicating for value,” Yorktown, NY (*February 2007*).
- “Basic Blue” IBM management training, Armonk, NY (*December 2004*).
- “Leadership Development Program” offered by Leadership Education for Asia Pacifics, Southbury, CT (*October 2004*).
- IBM “President’s Class,” Atlanta, GA (*May 1997*).
- “Effectiveness skills: operating in the political dimension” (*March 1996*).
- IBM “Low Power Workshop” (*Fall 1994*).
- “The seven habits of highly effective people” (*Fall 1994*).
- “Self assessment for career management” (*Summer 1992*).
- “Understanding the silicon bipolar transistor” (*Fall 1990*).
- “Principles of object-oriented computing” (*Spring 1990*).

Organized an eleven-part technical seminar series in the summer of 1990.

Assisted in co-ordination of printers, workstations, UNIX installation and maintenance in the department; participated in a task force to make recommendations on equipment/software procurement and maintenance policies.

Supervised the following graduate summer interns:

- Yiyu Shi, University of California at Los Angeles (*2007*)
- Hanif Fatemi, University of Southern California (*2006 and 2007*)
- Ruiming Chen, Northwestern University (*2006*)
- Irene Dhong, Johns Hopkins (*2005*)
- Jinjun Xiong, University of California at Los Angeles (*2005*)
- Lizheng Zhang, University of Wisconsin at Madison (*2005*)
- Hongliang Chang, University of Minnesota (*2004*)
- Kaushik Ravindran, University of California at Berkeley (*2003*)

- Dinesh D. Patil, Stanford University (co-supervised with S. Kosonocky, *2003*)
- Srinath R. Naidu, Eindhoven University of Technology (*2002*)
- Xiaoliang Bai, University of California at San Diego (*2001*)
- Luís G. Silva, Technical University of Lisbon (*1999*)
- Payam Heydari, University of Southern California (*1998*)
- Etienne T. A. F. Jacobs, Eindhoven University (*1997*)
- Naresh Maheswari, Iowa State University (*1996*)
- Lance Hester, Northwestern University (*1995*)
- Florin Dartu, Carnegie Mellon University (*1994*)
- Dennis Ciplickas, Carnegie Mellon University (*1993*)
- Anirudh Devgan, Carnegie Mellon University (*1992*)
- Ronald Braunstein, University of California at Berkeley (*1991*)
- Jalal A. Wehbeh, University of Illinois (*1990 and 1991*).

**STATUS AND  
ACTIVITIES**

Citizen of the United States.

Fellow, IEEE.

Member, Union of Concerned Scientists.

Frisbee, pool, crossword puzzles, music, skiing, tennis, travel, fiction.

Founder editor of a campus magazine, "SPECTATOR," (*7/1981 - 6/1982*).

Member, University debate team, (*7/1981 - 6/1985*).

Recipient of University Colors for literary activities (*5/1985*).