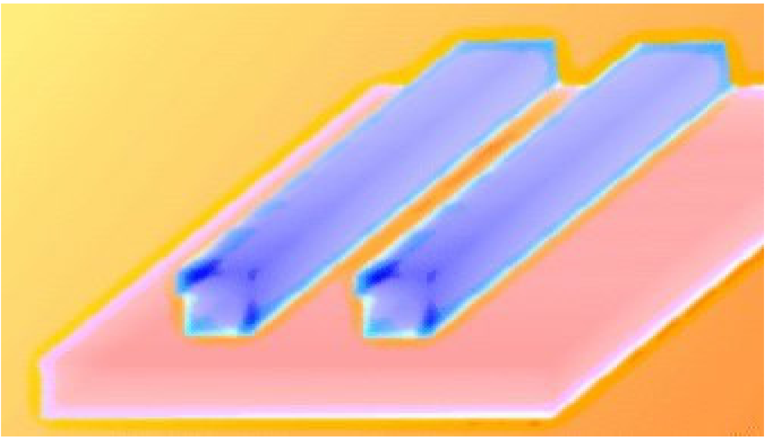
On-chip Interconnect: Design and Modeling Methodology



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IBM Burlington Design Automation Enablement

Major events

- **June 1998 –** Research starts at IBM Haifa Research Labs
- **January 2000 –** Start of joint work with MD (Burlington) Design Automation Department
- **January 2001 –** T-line Geometries + models inside IBM Design kit
- **December 2002 –** IBM Research Accomplishment Award
- **Up to January 2005 –** 8 IEEE papers published + 5 patents filed (more already submitted)

Wiring for high speed on-chip design: methodology gap

Analog & mixed signal design methodology is not adequate

- For high frequency design, post-layout wiring analysis is usually too late
- State of the art in wiring extraction is mostly RC. But: even around 1GHz, inductance starts to impact longer wires behavior
- The attempts to develop RCL post-layout extraction methods usually fail, due to inability to determine the correct current return paths
- The existing extraction tools do not take into account several important physical effects, such as substrate effects

Microwave design methodology is not adequate as well

- Traditional microwave concepts (each wire is critical, impedance matching of each element) are not applicable for many A&MS designs
- Fully nonlinear, large signal transient SPICE simulations required
- Mixed signal simulations required

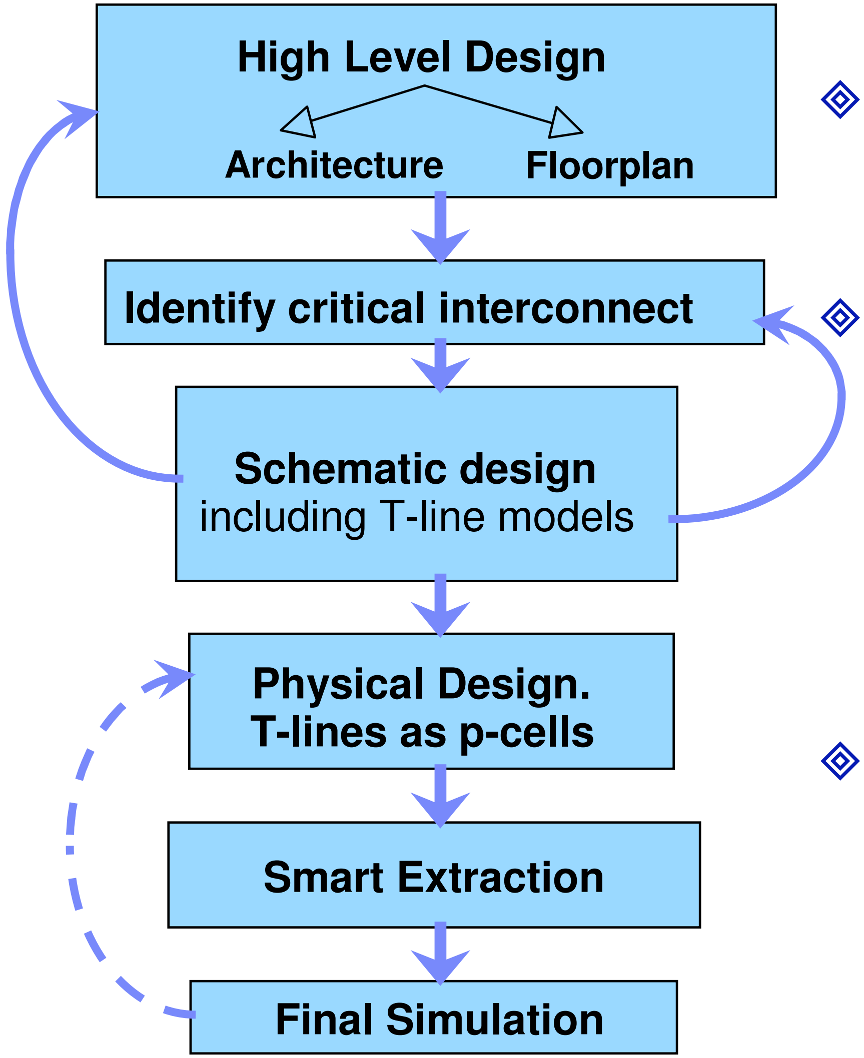
Proposed solution :

T-line devices as design components for critical on-chip wires

"Combine design automation with designer's wisdom!"

- **Design of critical wires** rather than extraction
- Use **predefined T-line geometries** as parameterized design templates
- **Support the specific technology** details (given metal stack, copper..)
- **Semi-analytical** time & frequency domain **models** optimized for the specific technology bandwidth **(today from DC up to 200 GHz)**
- Easy usage in **different circuit simulators** and design environments
- Support **all simulation kinds**: transient, AC, PSS, S-param, mixed-mode
- Easy **custom modeling** for specific designs (HSS, RFICs).

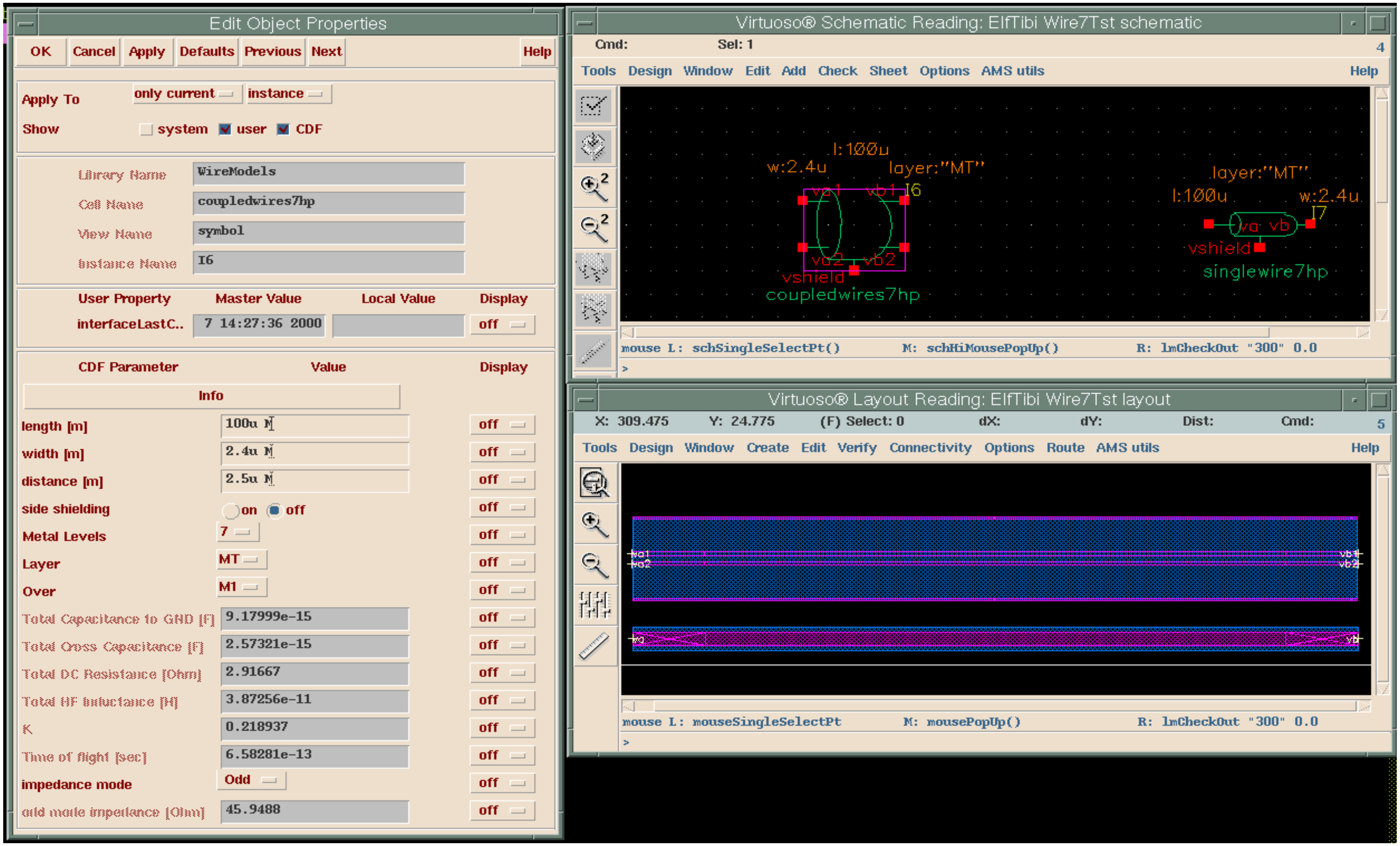
The interconnect-aware design flow
(patent filed)



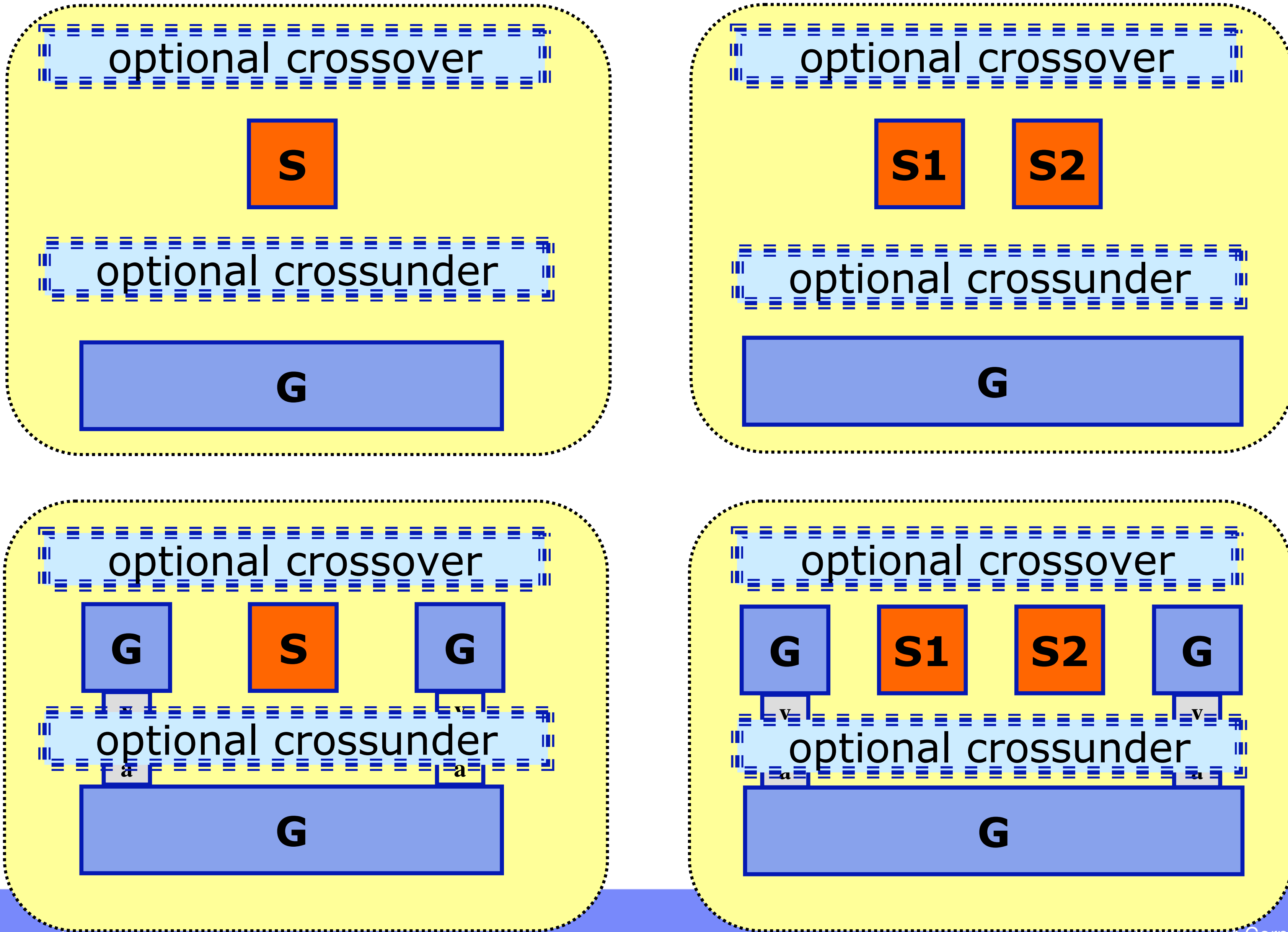
- **Sorting wires into 2 groups:**
  - **critical, small group**
  - **non-critical, most of the wires**
- **Design of critical wires:**
  - **Predefined set of parametrized T-line structures as design components**
  - **Pcell based: T-line device = symbol+schematic+layout views**
  - **DRC and LVS clean layout**
  - **Monitoring T-line parameters is enabled**
- **Smart extraction**
  - **Use T-line models for critical wires**
  - **Use RC extract for non-critical wiring - sufficient accuracy**
  - **Back-annotate final T-lines parameters**

Vision: On-chip T- lines become an industry standard

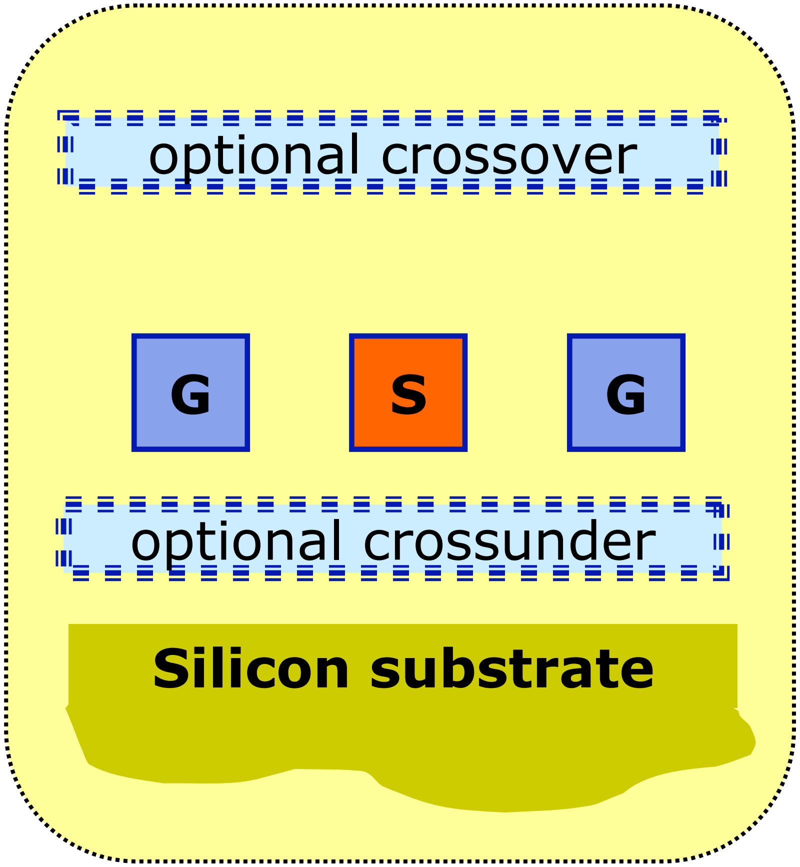
IBM sample T-line model interface in Cadence environment

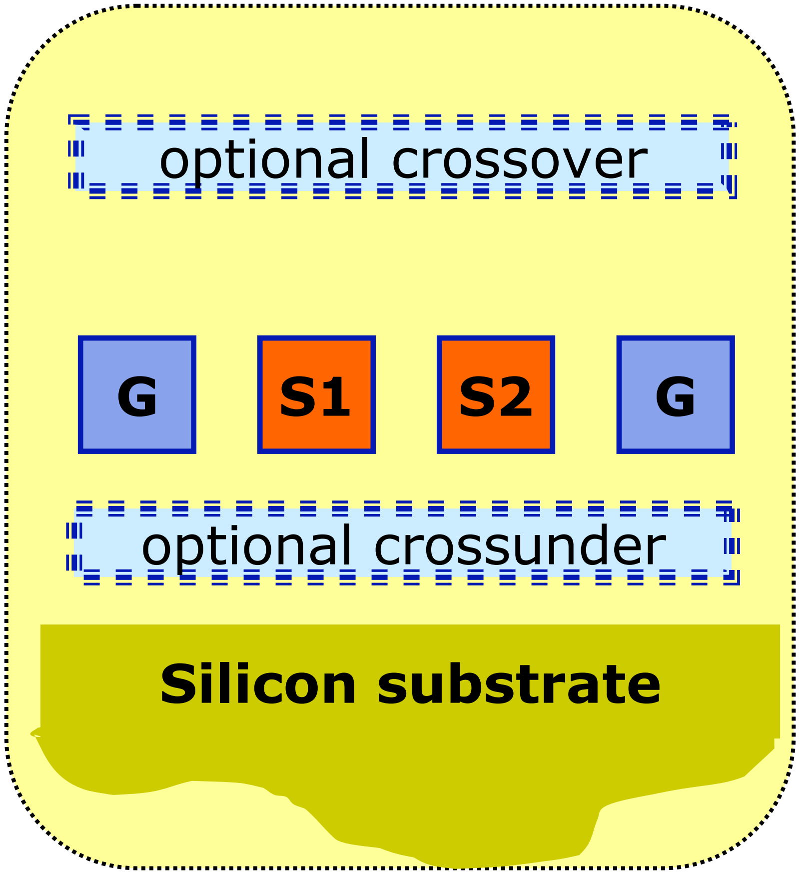


Microstrip T-lines

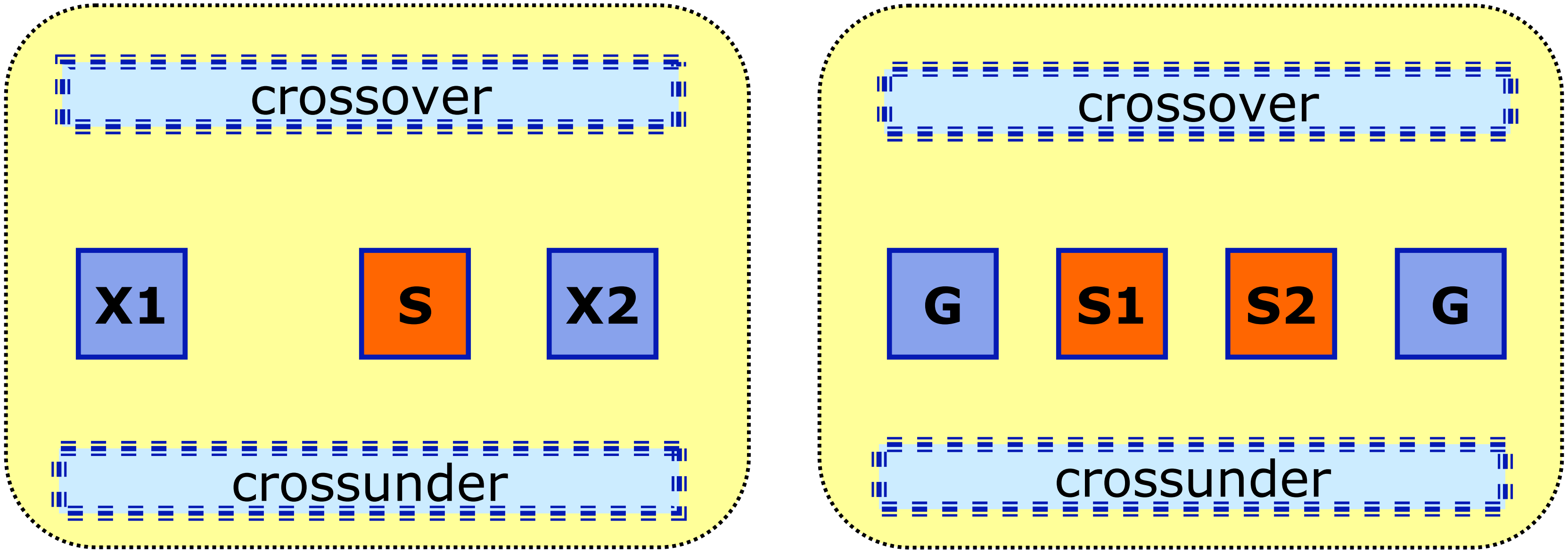


Coplanar T-lines





RC Lines



User can define each of the neighbors X1, X2 as:

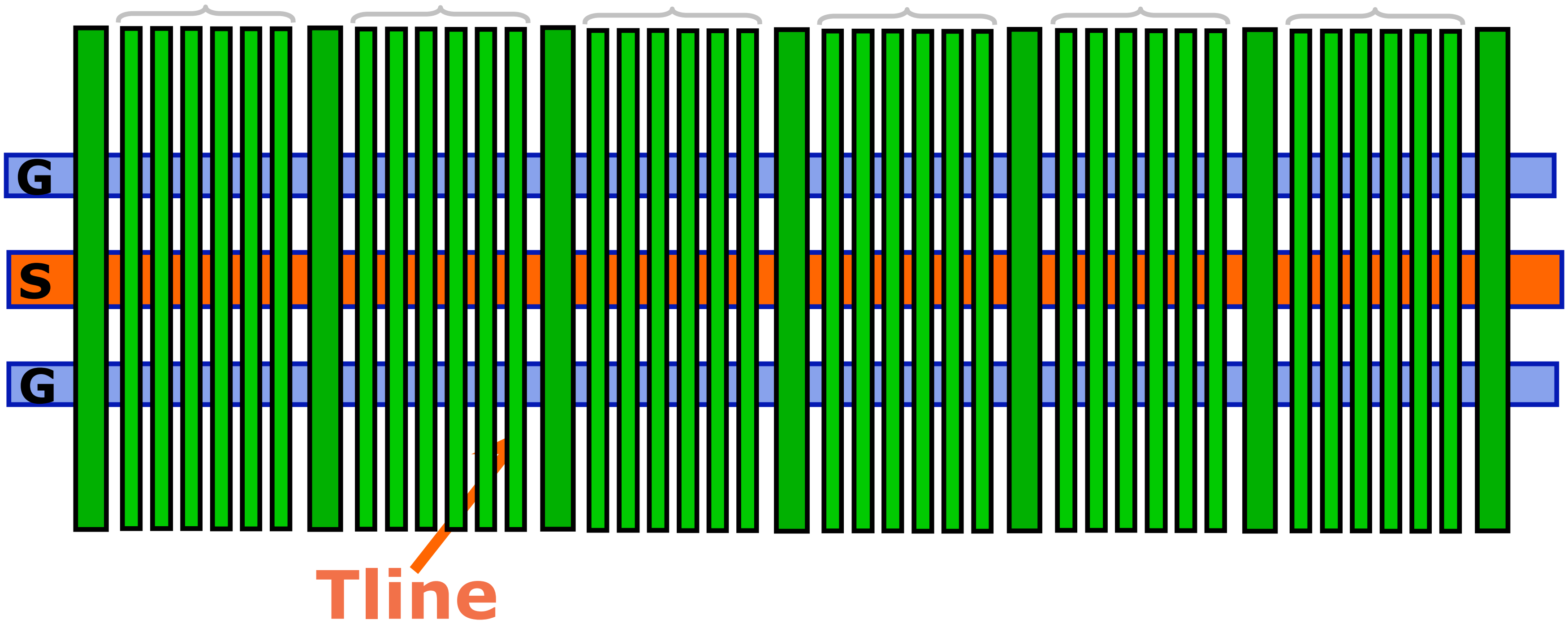
"Quiet": the neighbor is grounded

"Friendly": the neighbor's voltage is identical to that of the signal wire

"Hostile": the neighbor's voltage is opposite to that of the signal wire (the same frequency and amplitude, but opposite phase)

Crossing lines cases

Example: Single coplanar T-line with crossing from above (crossover)



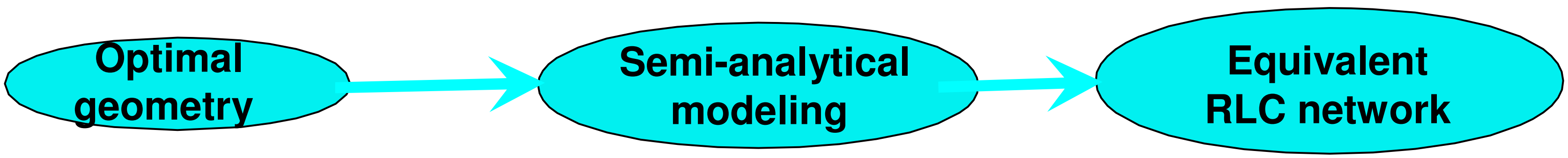
Digital applications: Dense crossing in adjacent layers above & below

A&MS applications: Dense/sparse crossing in various metal layers

IBM on-chip T-line modeling

Previous approaches:

- Trying to solve undefined electromagnetic environment
- Mainly numerical technique (convergence, time & accuracy problems)
- Many suffer from stability problems



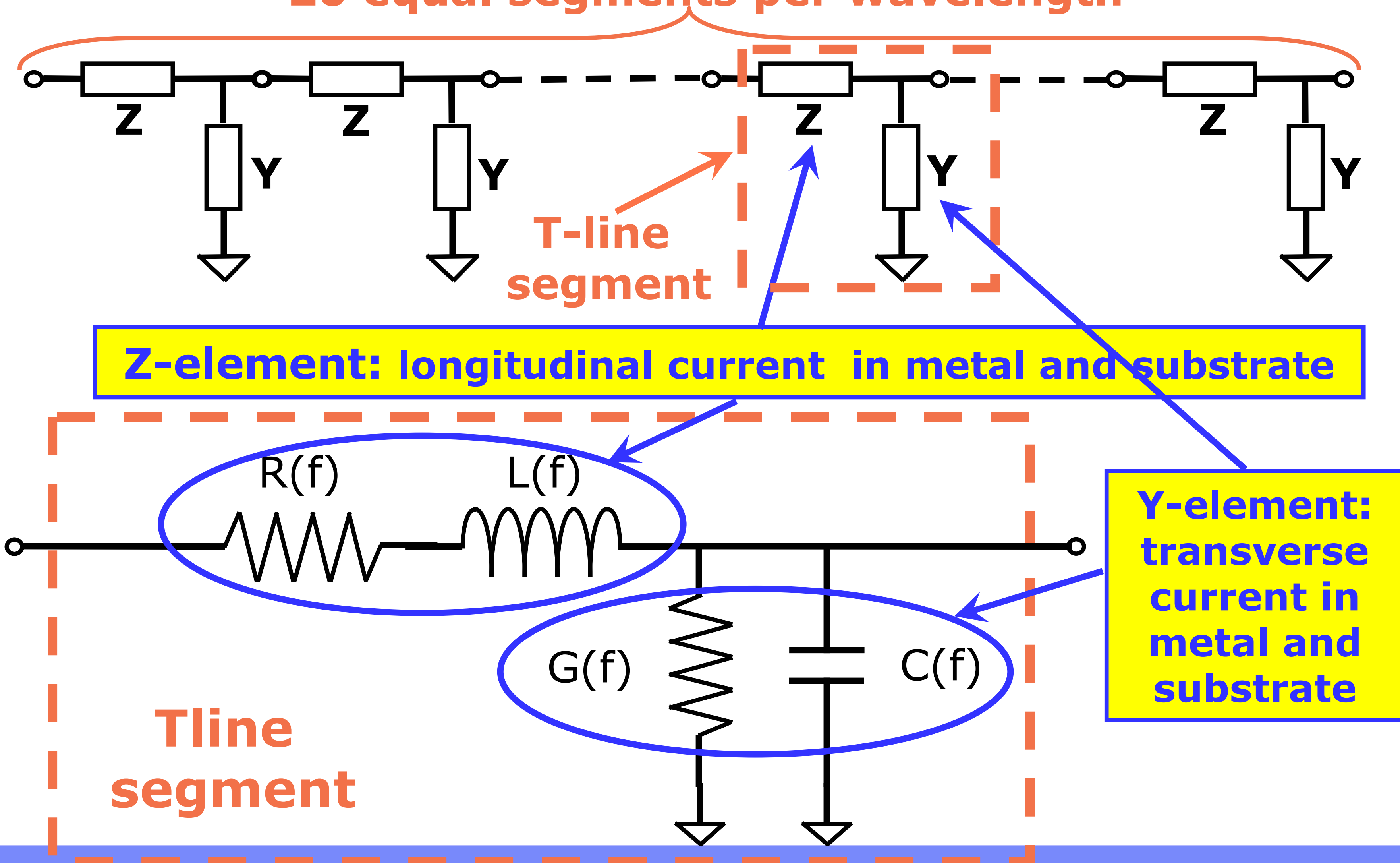
Our approach:

- Closed electromagnetic environment ensured by T- lines design
- Only physics- based semi-analytical explicit expressions
- Inherent passivity => stability

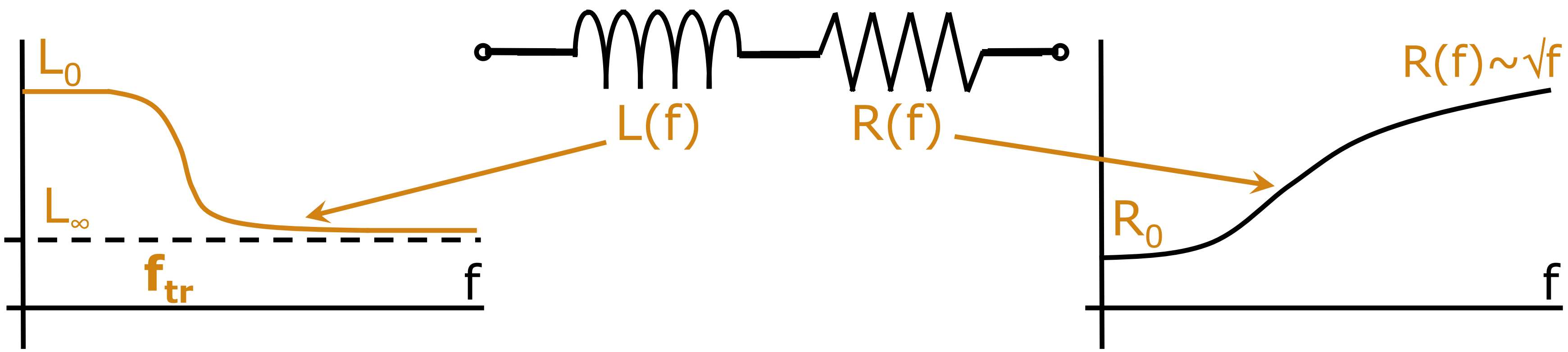
Modeling technique:

ZY-network

~20 equal segments per wavelength



Modeling the Z-element: problem description

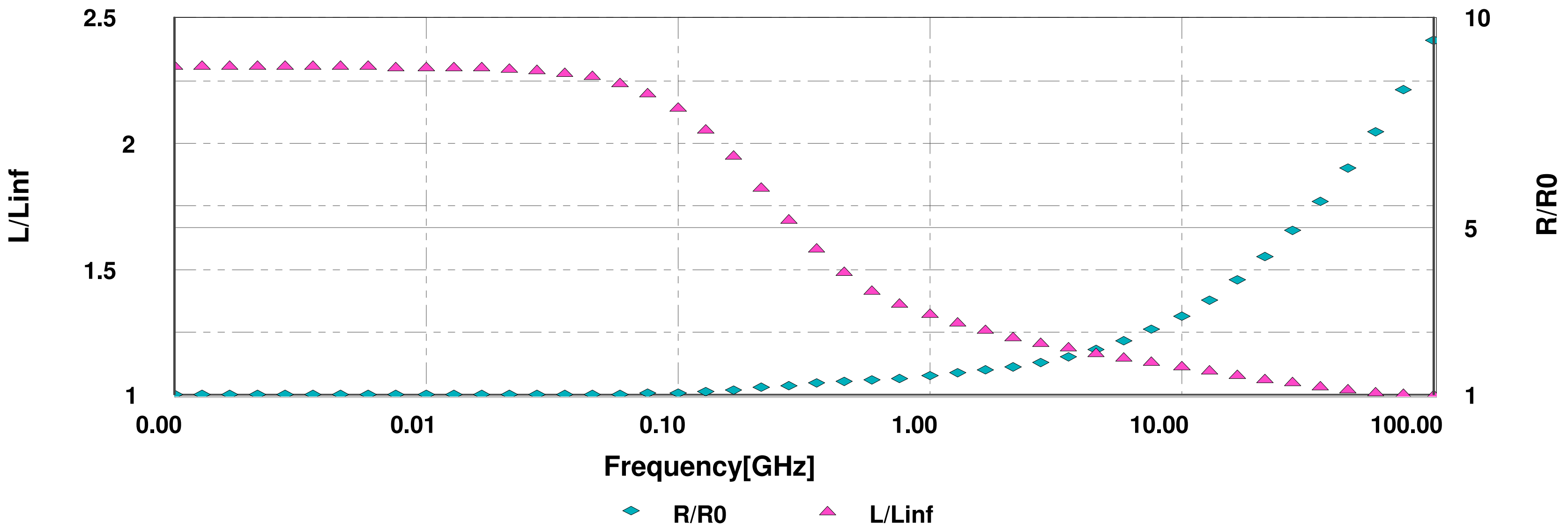


f_{tr} : transition frequency, at which the skin depth is comparable with relevant cross-section dimensions

$f << f_{tr}$:the current is uniformly distributed in all the metal cross-sections

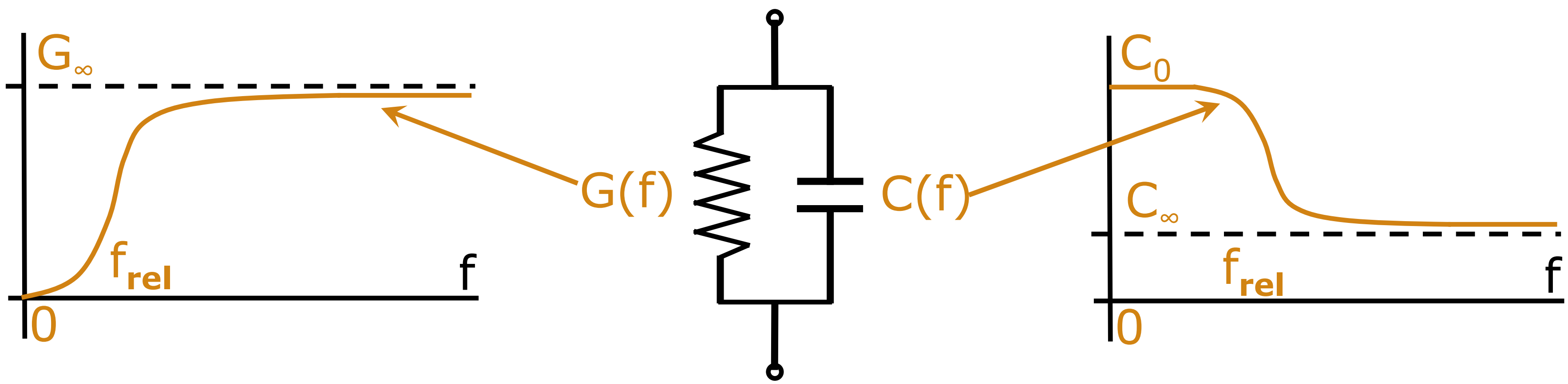
$f >> f_{tr}$:the current is non uniformly distributed at the surface of the metals

R(f), L(f) and Zo(f) of a typical Microstrip T-line in commonly used top metal layer (Aluminum, 4um thick)



f [Hz]	R [Ohm/mm]	L [nH/mm]	Zo [Ohm]
DC	1.255	0.798	undefined
1G	1.71	0.384	51 - 16.3 J
10G	3.33	0.331	45.1 - 3.59 J
60G	8.29	0.303	43

Modeling the Y- element: problem description

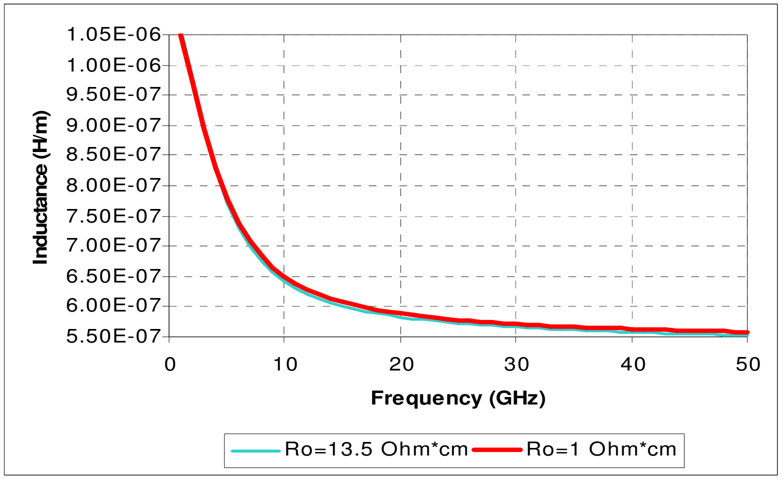


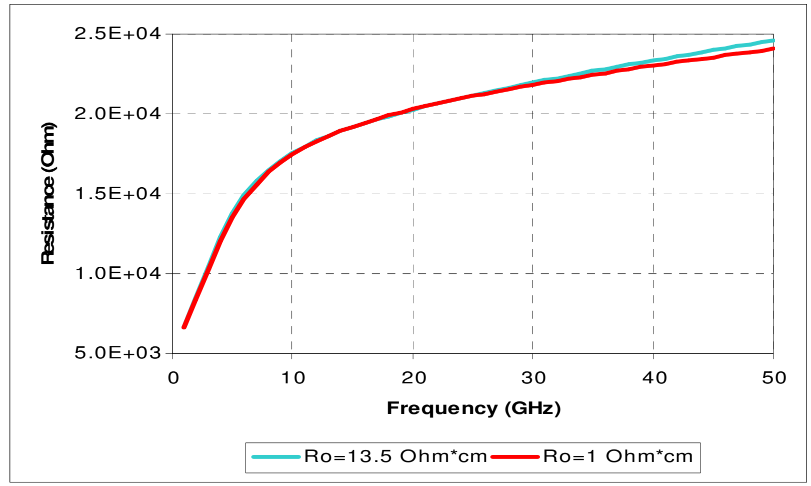
$$f_{rel} = \frac{1}{2\pi}\frac{\sigma_s}{\varepsilon_s}$$

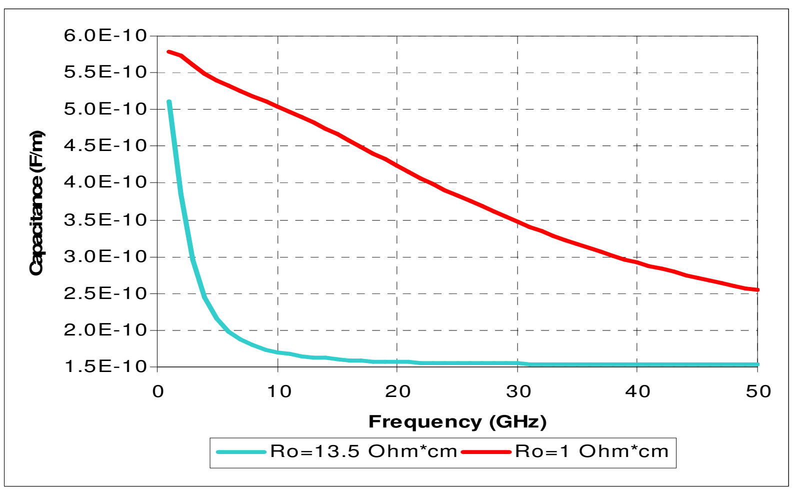
$f << f_{rel}$:the substrate behaves as an ideal metal

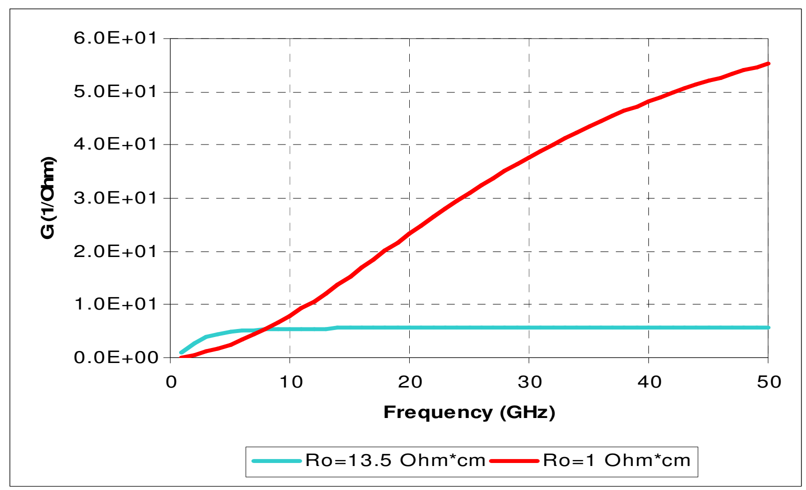
$f >> f_{rel}$:the electric field in the silicon substrate is the same as it would be for an ideal dielectric

HFSS Result: Single T-line, M1/sub, w=s=ws=6um
L(f), R(f), C(f),G(f) for ρ_{sub}=1 Ohm*cm, 13.5 Ohm*cm

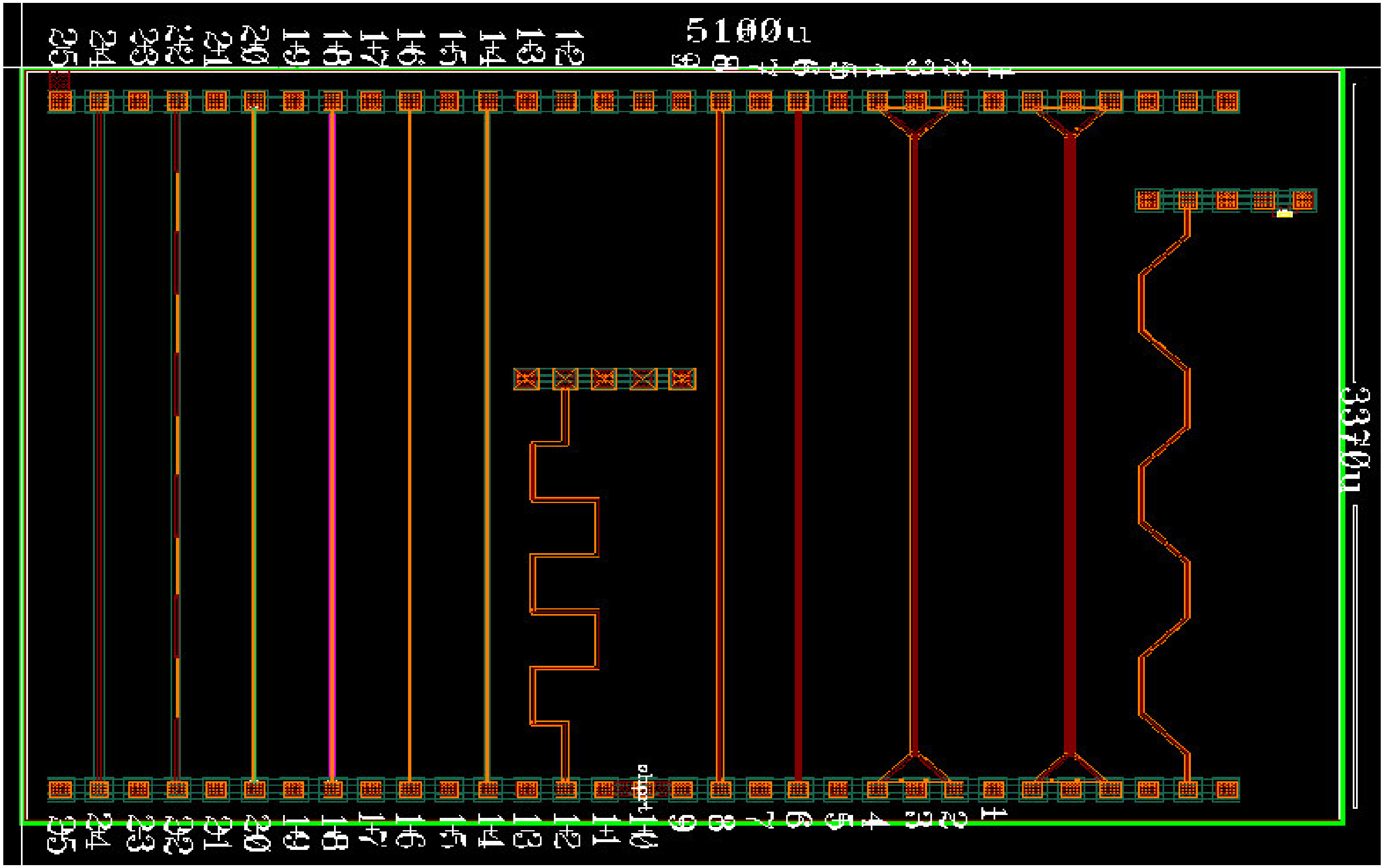




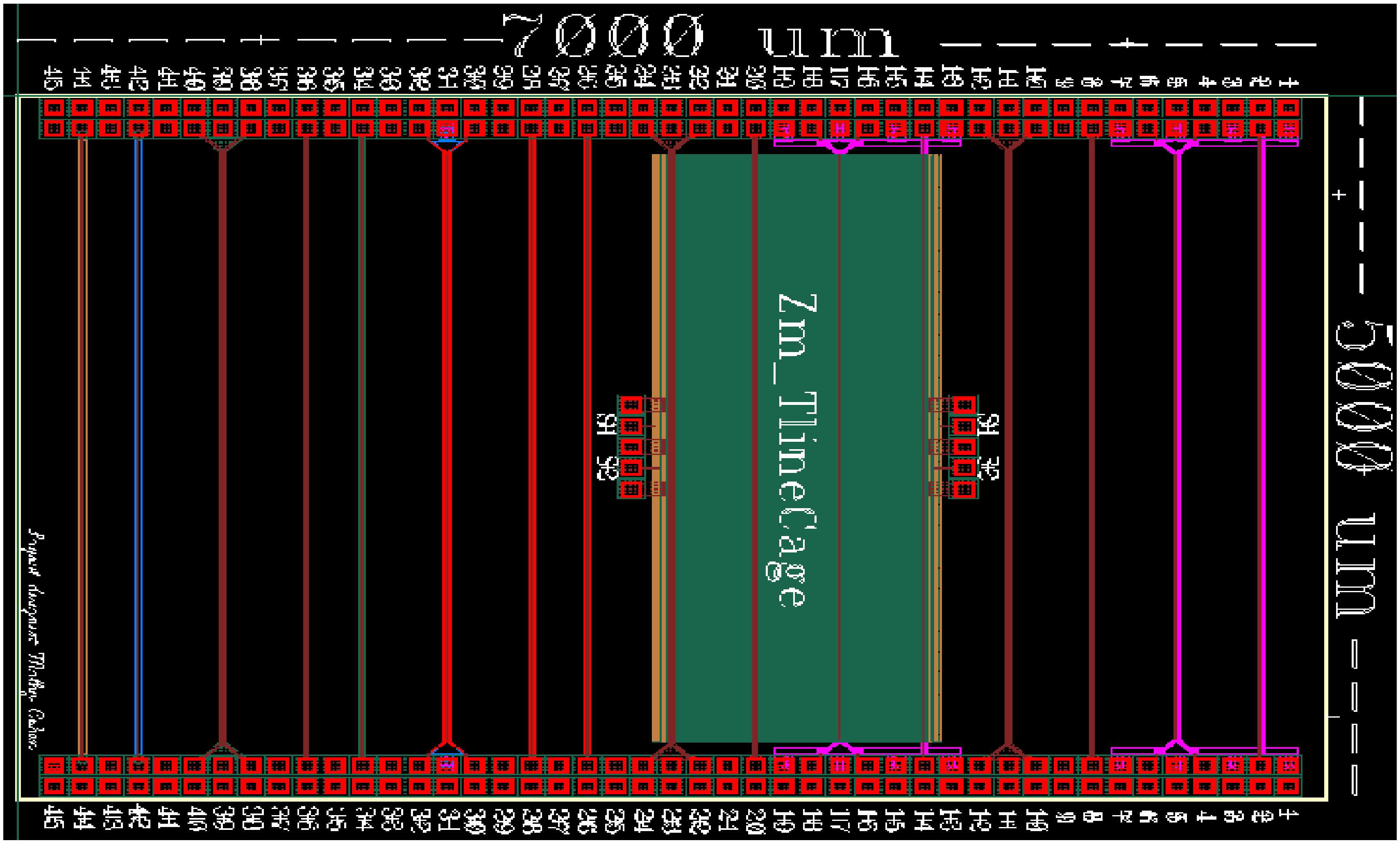




On-chip microstrip T-line test cage



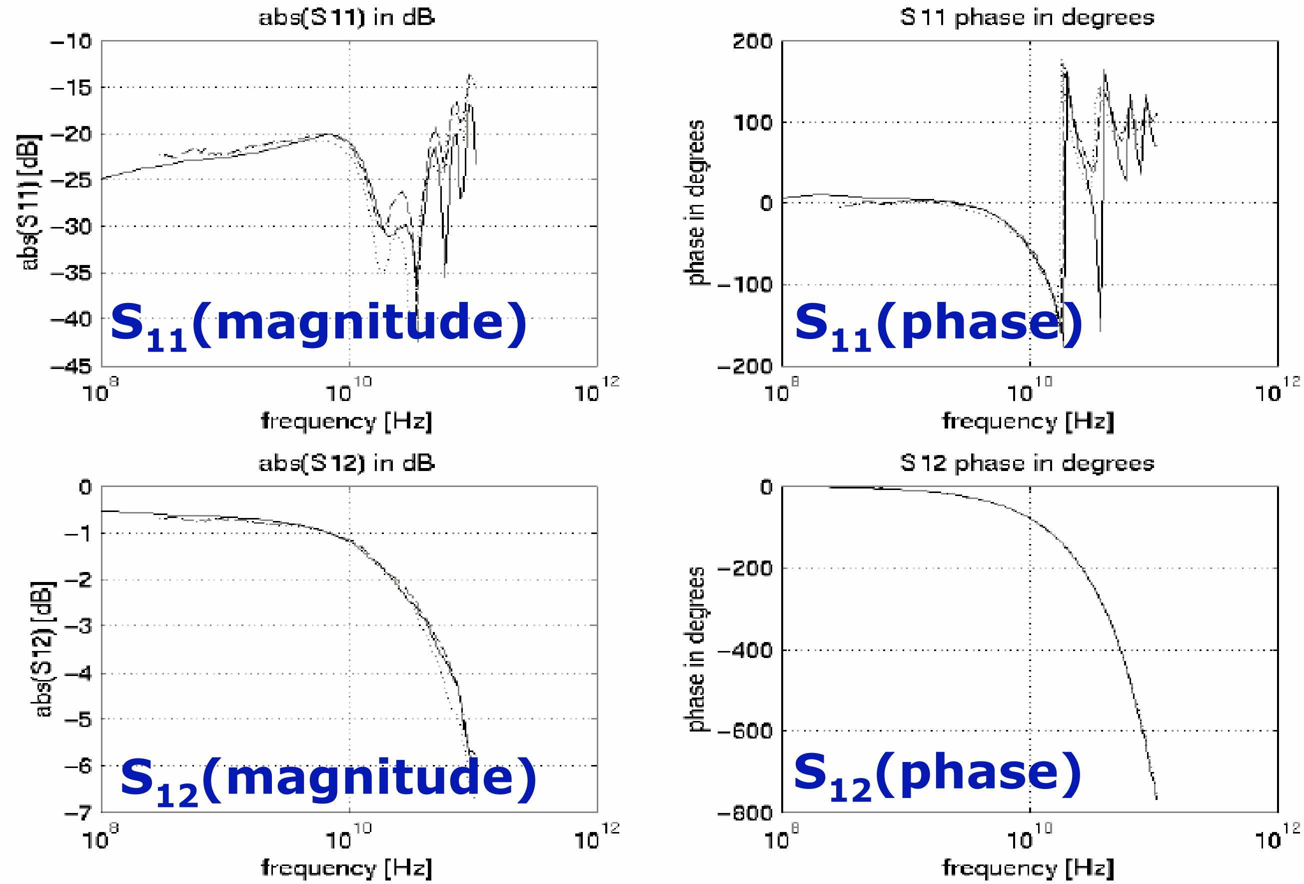
Microstrip & coplanar T-lines with crossing lines



Hardware measurements setup

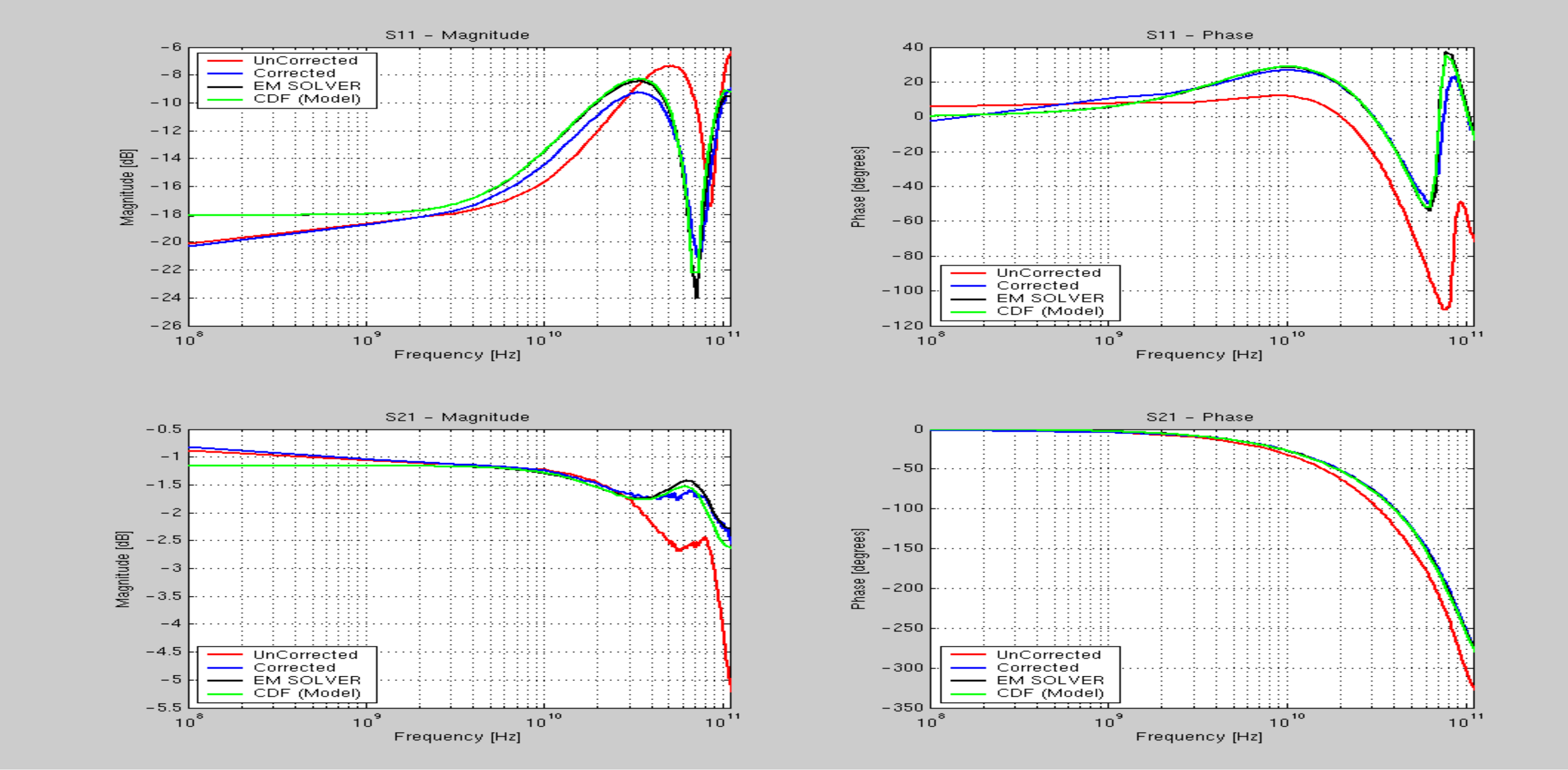
- 2 independent measurement sessions performed in IBM Haifa and Burlington on different units of the same test chip
- IBM Burlington: Agilent HP8510XF 110GHz 2-port Vector Network Analyzer, used for single T-lines; LRRM calibration on standard alumina substrate
- IBM Haifa: Agilent 8720ES 20GHz 4-port Vector Network Analyzer with an ATN-4112A unit, used for both single and coupled T-lines; SOLT calibration on standard alumina substrate
- Balanced (GSG & GSGSG) coplanar probes used in both IBM sites
- Combined Y and Z-parameter parasitics de-embedding for bottom shielded on-chip pads in IBM sites

Measured S-parameters of bent T-line structures versus their straight reference



Dashed: 45º bends, dotted: 90º bends, solid: straight line

S-parameters of a single T-line



Green: model Blue: 110 GHz measurement,
Black: EM solvers Red: raw measurement (no pad de-embedding)

Patents/Publications

1) Patent filed: David Goren et al, "An Interconnect-Aware Methodology for Integrated Circuit Design", Pat. No. 10/091,934 filed March 6 (2002)
2) Patent filed: Rachel Gordin, David Goren and Michael Zelikson "Interconnect-Aware integrated circuit design" Pat. No. 10/723,752 filed November 26 2003.
3) Patent filed: Rachel Gordin and David Goren, "Modeling Capacitance of On-Chip Coplanar Transmission Lines over the Silicon Substrate"
4) Patent filed: David Goren et al, "Device and method for reducing dishing of critical on-chip interconnect lines", Pat. No. 10/954,672, filed 30 September 2004
5) Patent filed: David Goren et al, "Integrated Circuit Transformer Devices for On-Chip Millimeter-Wave Applications", filed as docket YOR920040637US1
6) D. Goren et al, "An Interconnect-Aware Methodology for Analog and Mixed Signal Design, Based on High Bandwidth (Over 40GHz) on-chip Transmission Line Approach", IEEE DATE02 Conference, Paris, March (2002).
7) R. Gordin, D. Goren and M. Zelikson, "Modeling of On-Chip Transmission Lines in High Speed A&MS Design - The Low Frequency Inductance Calculation", IEEE Signal Propagation On Interconnects Conference, Pisa, May (2002).

More Patents/Publications

7) D. Goren, M. Zelikson and R. Gordin, "Interconnect-Aware Design Methodology for Analog and Mixed Signal Design in Silicon Based Technologies using High Bandwidth On-Chip Transmission Lines", IEEE 2002 conference in Israel.

8) D. Goren, Rachel Gordin and Michael Zelikson, "Modeling Methodology for On-Chip Coplanar Transmission Lines over the Lossy Silicon Substrate", IEEE Signal Propagation on Interconnects conference, Siena (2003).

9) R. Gordin, D. Goren and M. Zelikson, "Study of On-Chip Coplanar Transmission Lines over the Lossy Silicon Substrate", IEEE Signal Propagation on Interconnects conference, Siena (2003).

10) D. Goren et al, "On-Chip Interconnect-Aware Design and Modeling Methodology, based on High Bandwidth Transmission Line Devices", IEEE DAC 2003 conference, Anaheim 2003.

11) R. Gordin and D. Goren, "Modeling Capacitance of On-Chip Coplanar Transmission Lines over the Silicon Substrate ", IEEE Signal Propagation on Interconnects Conference (2004).

12) Thomas Zwick, Youri Tretiakov and David Goren, On-Chip Transmission Line Measurement and Modeling in IBMs SiGe Technology up to 110GHz, IEEE Microwave and Wireless Components Letters

Backup foils

Estimation of dense crossing line effects

The Full plane crossing approach:

- Full, solid metal plane is assumed as the crossing line layer (100% density) Good approximation if and when the distance to the crossing layer is larger than the separation between the crossing lines.
- Optionally above and/or below the signal line – in all metal stack layers.
- Implemented in all our T-line types (coplanar and microstrip).
- Crossing lines are all assumed to be grounded (like the T-line bottom/side shielding). This is a good approximation for all normally loaded quiet crossing lines – regardless of their load.
- Does not consider active (aggressor) crossing signals – or assumes that they cancel each other in normal operation (good assumption for differential signaling).
- Additional percentage input, which interpolates the crossing line effect between zero crossing and full plane crossing – for the less dense crossing cases.

Calculation of sparse/exact crossing line effects

Custom crossing:

- The user **inputs** the total capacitance per unit length due to **both** the T-line and the crossing lines – based on either static 3D EM solver (accepts AQUAIA/Emitpkg output) or the existing RC extraction tool.
- Intended for low density or non-uniform crossing.
- Potentially gives the exact result in critical cases (high level clock distribution, main high speed busses…)
- Implemented in all our T-line types (coplanar and microstrip).
- Crossing lines are all assumed to be grounded (like the T-line bottom/side shielding). This is a good approximation for all normally loaded quiet crossing lines – regardless of their load
- Does not consider active (aggressor) crossing signals – or assumes that they cancel each other in normal operation (good assumption for differential signaling).

Silicon substrate losses consideration in coplanar T-lines with crossing lines

- The silicon substrate effect on both the T-line losses, slow wave effect and frequency dependent capacitance are modeled in single and coupled coplanar T-lines without any crossing lines up to 100[GHz].
- Full Plane crossing options consider the effect of the silicon substrate in all cases. Crossunder cancels the silicon effects.
- Custom crossing includes a “Y/N” user option to consider the silicon effects:
  “Y” = No crossing exists from below
  “N” = Full density crossing exists from below
  The user can check the difference in his design case.