



**Chip(x)**

**Innovative ASIC Development  
Methodology to Significantly  
Reduce Time to Market**

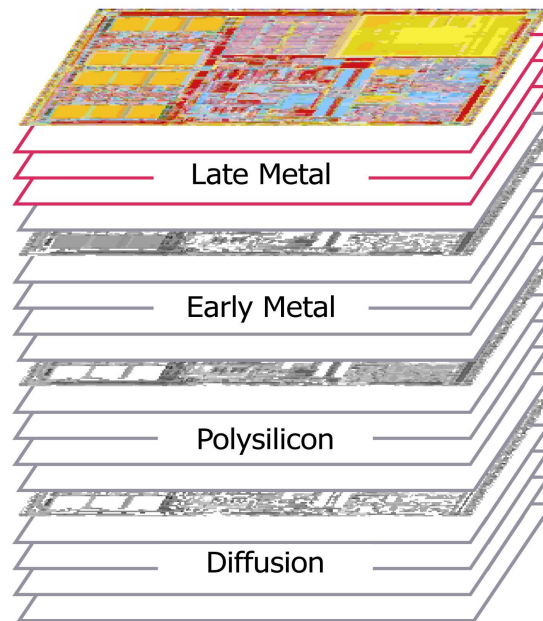
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VP of Engineering**



# Structured ASIC

## Standard Cell ASIC

Customer specific layers



## Structured ASIC

Customer specific layers

**Common layers:**

- Logic, Memory
- Configurable IO
- PHY, PLL, DLL
- DFT, Clock Trees
- Misc. IP
- Analog

1. **Fast Time to Market:**
2. **Very Low NRE:**
3. **Low Risk:**
4. **ASIC Performance:**

Prototypes in 6-7 weeks from hand-off  
As little as \$25K  
Pre-built IP, clock trees, analog  
Over 300MHz in 0.13 $\mu$



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## Flexible Building Blocks

- ◆ Logic gate library
- ◆ IO library
- ◆ RAM library
- ◆ PLL, DLL, CDL
- ◆ Integrated SerDes: 1Gz to 3.125Gz
- ◆ PCIe Phy and Controller
- ◆ USB 2.0 OTG Phy
- ◆ DDR-I/II phy interface



# ChipX Structured ASIC Advantages

- ◆ Offer a low-risk alternative to Standard Cell ASICs
- ◆ Offer a low-cost alternative to FPGAs
- ◆ Provide mixed signal SOC platform solution
- ◆ Take care of power optimization, cross talk effects, signal integrity, timing closure in advance  
=> Shorten development cycle
- ◆ Enable fast and low cost re-spins of the silicon using metal layers only

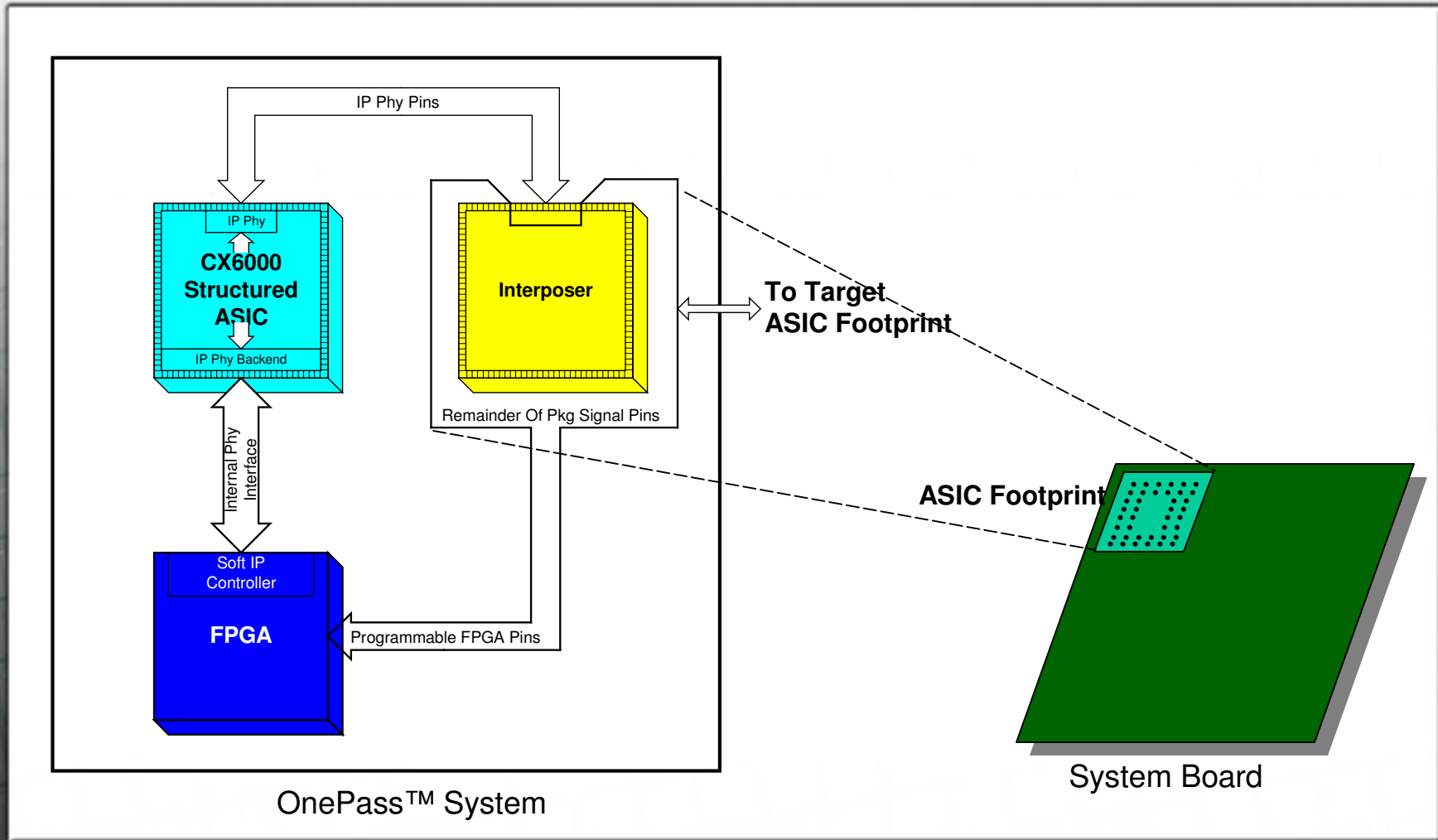


## Verification Problem Definition

- ◆ **Optimizing system development time is extremely important to you.**
  - Traditional simulations take a very long time
- ◆ **FPGAs help you prototype your system quickly but forces you to build two different H/W platforms**
- ◆ **You want the performance of an ASIC but system verification is your biggest bottleneck**
- ◆ **Converting from an FPGA to an ASIC is time consuming and can be risky if mixed signal is involved**



# OnePass™ System





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## What is OnePass™?

- ◆ OnePass™ is a **conversion-less** ASIC design and verification system for ChipX CX6000 (0.13μ) products
  - Leverages **the flexibility of FPGAs**
  - Fits in the **same footprint** as the final ASIC
  - Uses the **same PHY** as the Structured ASIC base array, eliminating the risk of mixed signal integration
- ◆ **Software development begins early using system hardware**
  - Parallel S/W development and system validation with SA fabrication → **ASIC TTM ~ FPGA TTM**



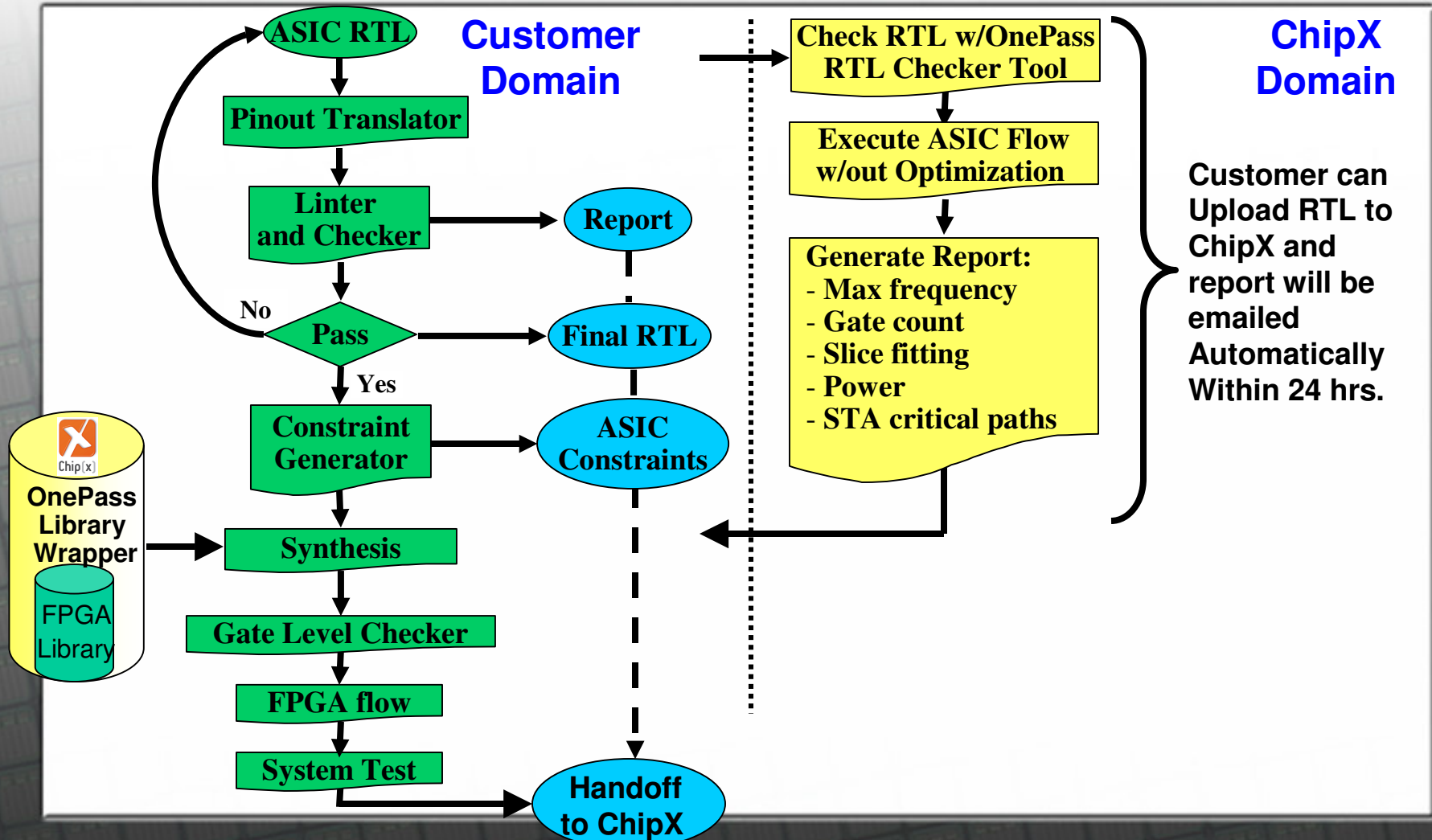
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## What is OnePass™?

- ◆ Eliminates **time consuming** and **risky** conversion
- ◆ Insures that final design will **fit** in the ASIC of choice
- ◆ Uses the optimum package from day one to **accelerate development** and **save board and package cost**



# OnePass™ Development Flow





## Summary of OnePass™ Benefits

- ✓ **No design conversion necessary**
- ✓ **One flow for both FPGA and ASIC development**
- ✓ **All ASIC requirements generated during flow**
- ✓ **Automatic pre-processing of design by ChipX to provide vital information to customer. Operation can be repeated as often as needed**
- ✓ **Most timing issues addressed up front**
- ✓ **Guarantee that design will fit in ASIC**
- ✓ **Short backend processing time – Two to Four weeks from final RTL to Tape Out.**