



## HVC 2012 - Agenda

### November 6 – Day 1

<p><b>09:00</b> Registration</p> <p><b>09:30</b> Opening Remarks <i>Oded Cohn, Director, IBM Research – Haifa</i></p> <p><b>10:00</b> <b>Keynote Speaker: On Behavioral Programming</b> <i>Prof. David Harel, Weizmann Institute of Science</i></p> <p><i>Session Chair: João Lourenço, New University of Lisbon</i></p> <p><b>11:00</b> Break</p> <p><b>11:30</b> <b>Technical Session 1: Software Testing and Verification</b> <i>Session Chair: Eran Yahav, Technion</i></p> <p><b>11:30</b> Precise Detection of Atomicity Violations (<b>Winner of the Best Paper Award</b>) <i>Vasco Pessanha, Ricardo Dias, and João Lourenço</i></p> <p><b>12:00</b> Proving Mutual Termination of Programs <i>Dima Elenbogen, Shmuel Katz, and Ofer Strichman</i></p> <p><b>12:30</b> Knowledge-Based Transactional Behavior <i>Saddek Bensalem, Marius Bozga, Doron Peled, and Jean Quilbeuf</i></p> <p><b>13:00</b> Lunch</p>	<p><b>14:30</b> <b>Technical Session 2: Software Testing and Verification, Poster Promos</b> <i>Session Chair: Onn Shehory, IBM Research – Haifa</i></p> <p><b>14:30</b> (Tool Paper) FoREnSiC - An Automatic Debugging Environment for C Programs <i>Roderick Bloem, Rolf Drechsler, Goerschwin Fey, Alexander Finder, Georg Hofferek, Robert Koenighofer, Jaan Raik, Urmas Repinski, and Andre Suelflow</i></p> <p><b>14:45</b> Repair with On-the-fly Program Analysis <i>Robert Koenighofer and Roderick Bloem</i></p> <p><b>15:15</b> Poster Promos</p> <p><b>15:30</b> Break</p> <p><b>16:00</b> <b>Technical Session 3: SAT</b> <i>Session Chair: Ofer Strichman, Technion</i></p> <p><b>16:00</b> Computing Interpolants without Proofs <i>Alexander Ivrii, Arie Matsliah, and Hana Chockler</i></p> <p><b>16:30</b> MaxSAT-Based MCS Enumeration <i>Antonio Morgado, Mark Liffiton, and João Marques-Silva</i></p> <p><b>17:00</b> Automated Reencoding of Boolean Formulas <i>Norbert Manthey, Marijn Heule, and Armin Biere</i></p> <p><b>17:30</b> Reception and Posters</p>
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## HVC 2012 - Agenda

### November 7 – Day 2

<p><b>09:30 Keynote Speaker: Verifying Real-Time Software Is Not Reasonable (Today)</b> <i>Prof. Edward Lee, UC Berkeley</i></p> <p><i>Session Chair: Henry Broodney, IBM Research – Haifa</i></p>	<p><b>12:45</b> Lunch</p>
<p><b>10:30</b> Break</p>	<p><b>14:15 Technical Session 5: Systems Engineering</b> <i>Session Chair: Karen Yorav, IBM Research – Haifa</i></p>
<p><b>11:00 Technical Session 4: Hardware Verification and Validation</b> <i>Session Chair: Eli Singerman, Intel</i></p>	<p><b>14:15</b> Statistical Model Checking for Safety Critical Hybrid Systems: An Empirical Evaluation <i>Youngjoo Kim, Moonzoo Kim, and Taihyo Kim</i></p>
<p><b>11:00</b> Leveraging Accelerated Simulation for Floating-Point Regression <i>John Paul, Elena Guralnik, Anatoly Koyfman, Amir Nahir, and Subrat K Panda</i></p>	<p><b>14:45</b> A New Test Generation Methodology for System-level Verification of Production Processes <i>Tamer Salman, Allon Adir, Alex Goryachev, Lev Greenberg, and Gil Shurek</i></p>
<p><b>11:30</b> Coverage-based Trace Signal Selection for Fault Localisation in Post-Silicon Validation <i>Shucheng Zhu, Georg Weissenbacher, and Sharad Malik</i></p>	<p><b>15:15</b> Defining and Model Checking Abstractions of Complex Railway Models Using CSP  B <i>Faron Moller, Hoang Nga Nguyen, Markus Roggenbach, Steve Schneider, and Helen Treharne</i></p>
<p><b>12:00</b> A Novel Approach for Implementing Microarchitectural Verification Plans in Processor Designs <i>Yoav Katz, Michal Rimon, and Avi Ziv</i></p>	<p><b>15:45</b> Break</p>
<p><b>12:30</b> (Tool Paper) Towards Beneficial Hardware Acceleration in HAVEN: Evaluation of Testbed Architectures <i>Marcela Simkova and Ondrej Lengal</i></p>	<p><b>16:00 Invited Talk: Reducing Costs While Increasing Quality</b> <i>Dr. Orna Raz, IBM Research – Haifa</i></p> <p><i>Session Chair: Orna Grumberg, Technion</i></p>
	<p><b>17:00</b> Social Activity</p>



## HVC 2012 - Agenda

### November 8 – Day 3

<p><b>09:30</b> <b>Invited Talk: SMT in Verification, Modeling, and Testing at Microsoft</b> <i>Dr. Nikolaj Bjorner, Microsoft Research</i></p> <p><i>Session Chair: Armin Biere, Johannes Kepler University</i></p>	<p><b>13:00</b> Lunch</p>
<p><b>10:30</b> Break</p>	<p><b>14:00</b> <b>Technical Session 6: Formal Methods</b> <i>Session Chair: Sharad Malik, Princeton University</i></p>
<p><b>11:00</b> <b>Special Session on Security Verification</b> <i>Session Chair: Alex Goryachev, IBM Research – Haifa</i></p>	<p><b>14:00</b> Word Equations with Length Constraints: What's Decidable? <i>Vijay Ganesh, Mia Minnes, Armando Solar-Lezama, and Martin Rinard</i></p>
<p><b>11:00</b> A Vulnerability or a Bug? What's the Difference Anyway? Security Software Verification as Part of the Development Lifecycle <i>Ofer Maor, CTO, Quotium, and Global Membership Committee, OWASP</i></p>	<p><b>14:30</b> Environment-Friendly Safety <i>Orna Kupferman and Sigal Weiner</i></p>
<p><b>11:40</b> Formal Analysis of Security Data Paths in RTL Design <i>Jamil Mazzawi, Consulting Services Manager, Jasper Design Automation</i></p>	<p><b>15:00</b> Deterministic Compilation of Temporal Safety Properties in Explicit State Model Checking <i>Kristin Yvonne Rozier and Moshe Vardi</i></p>
<p><b>12:20</b> Simultaneous Information Flow Security and Circuit Redundancy in Boolean Gates <i>Prof. Ryan Kastner, University of California, San Diego</i></p>	<p><b>15:30</b> Break</p>
	<p><b>16:00</b> <b>Award Session</b></p> <p>HVC Best Paper Award</p>
	<p><b>16:15</b> HVC2012 Award: IC3 and Friends <i>Prof. Aaron Bradley, CU Boulder</i></p> <p>HVC2013 Kickoff</p>
	<p><b>17:30</b> Conclusion</p>