3rd HiPEAC Industrial Workshop on Compilers and Architectures

Call for Papers

April 17, 2007

Organized by the IBM Haifa Research Lab

Modern embedded architectures face a number of new challenges that are being introduced by technology limitations. Just a few of these challenges include ways to continue Moore's law in spite of the frequency wall and new methods to reduce power consumption. Despite these technology limitations, the embedded market still demands a continued increase in performance and a reduction in power consumption. Most of today's new embedded architectures introduce various types of parallelism to address these issues, including SIMD, SMT, SMP and multicore architectures. Some of the above parallelism in hardware is transparent to the end users but requires the compiler to better utilize the new features. Other directions rely on the users to guide the compiler and the system to utilize new hardware features. New dialects of current programming languages are needed and in some cases, new programming languages are required. This workshop will focus on these exciting new directions and how they are influencing the embedded architecture and compilation domain.

This seminar will be conducted jointly with the annual Compiler and Architecture seminar held in previous years (http://www.haifa.il.ibm.com/Workshops/compiler2005/index.html), and continues the series of HiPEAC Industrial Workshops (http://www.hipeac.net/industry_workshop2).

The official language of the workshop is English.

Topics

The main focus of this workshop is advanced embedded computer architecture and compiler technology. The topics of interest for this workshop include, but are not limited to:

- Modern embedded architectures and computational models
- Compilers and tools for modern embedded computer systems
- Multicore, multithreaded, superscalar, and VLIW architectures
- Compiler/hardware support for hiding memory latencies
- Support for correctness in embedded hardware and software (esp. with concurrency)
- Reconfigurable computing
- Dynamic translation and optimization
- I/O issues in parallel computing and their relation to applications
- Parallel programming languages, algorithms and applications
- Middleware and run time system support for parallel embedded computing
- High performance application specific systems
- Performance tools for embedded application behavior understanding
- Non-traditional embedded computing systems topics

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Important dates

February 16, 2007: Deadline for submission

March 6, 2007: Notification of paper acceptance

April 17, 2007: Workshop gathering and presentations

Submissions

Authors should submit their original contributions electronically to Ayal Zaks (zaks@il.ibm.com). Submissions must include an abstract. Please include your postal address, email, phone and fax numbers. An early email with your intention to submit a paper would be greatly appreciated. The authors are free to provide related documents (technical report, article) with additional details on their research work. The workshop will not have proceedings (abstracts will be provided online from http://www.hipeac.net/) so that presentation of already published work does not raise copyright issues.

While this workshop is organized by HiPEAC, submissions will be solely selected by researchers from the hosting industry. This time it will be done by researchers from IBM.

Contact Us

IBM Research Lab in Haifa, Israel (zaks@il.ibm.com)
http://www.haifa.il.ibm.com/dept/svt/code_compiler.html

Please feel free to further distribute this invitation to students and fellow researchers or developers.