Low Power Integrated Scan-Retention Mechanism

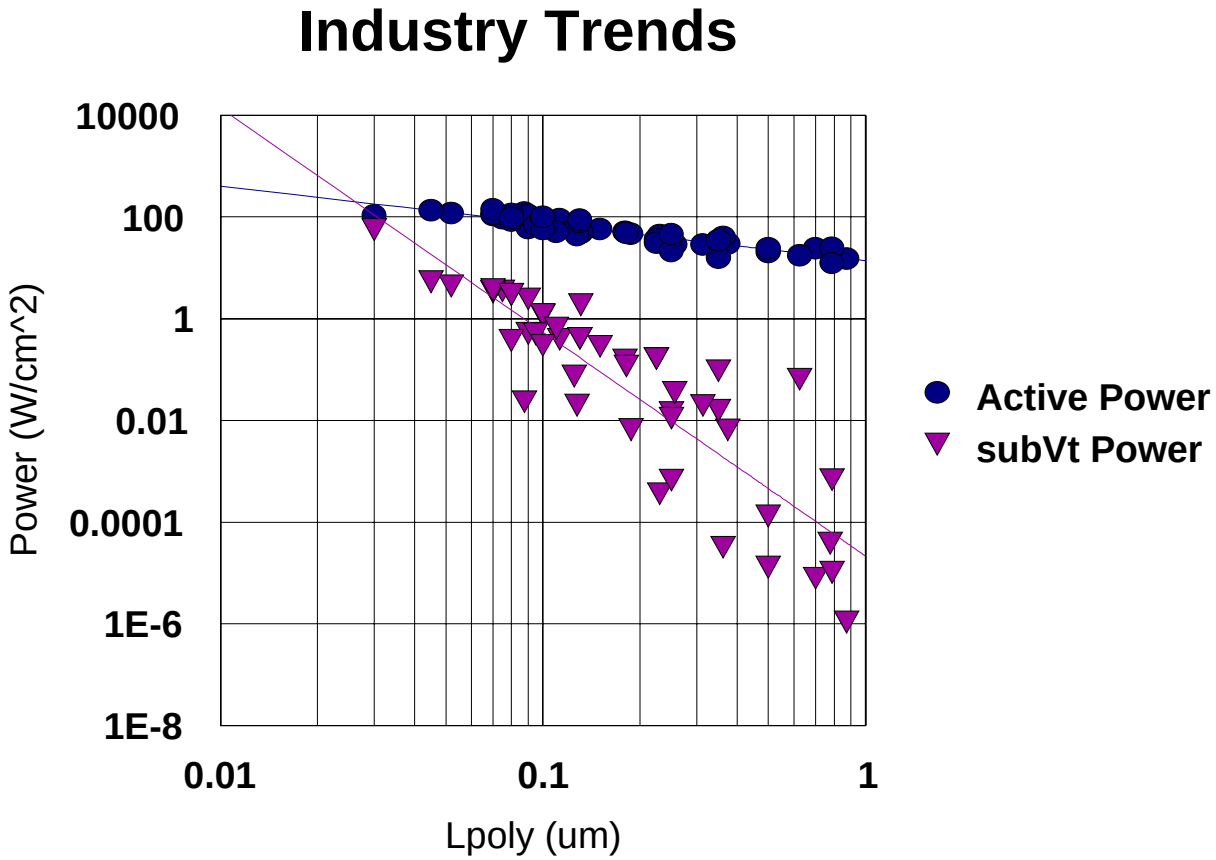
Victor V. Zyuban
Stephen V. Kosonocky

Acknowledgment to colleagues D. Knebel, G. Gristede, A. Haen, S. Kim and M. Immediato

Presentation Outline

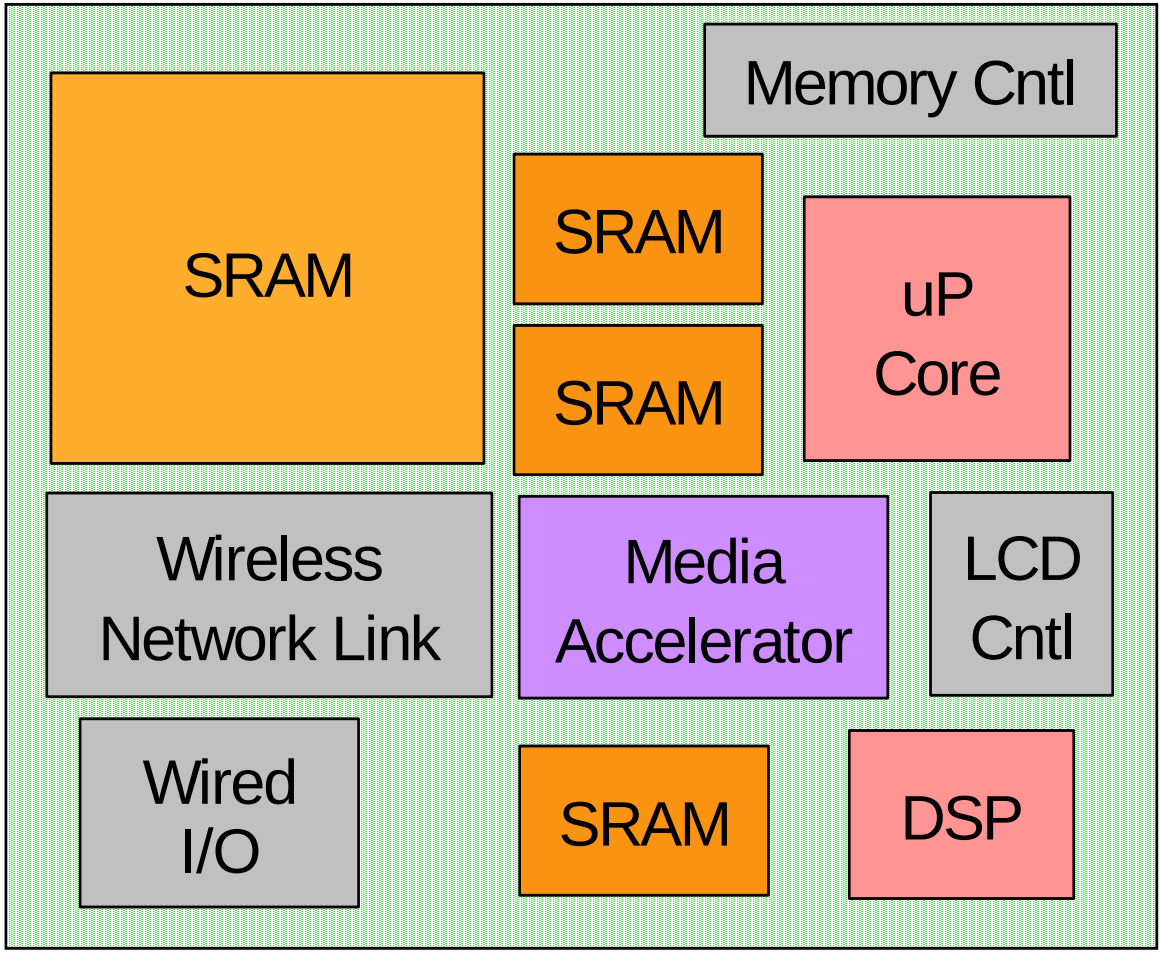
- Background
  - Give motivation for implementing power down mode.
  - Compare several approaches to saving state on power down.
  - Analyze power overhead of the prior art.
- Describe new low energy integrated scan-retention mechanism.
- Analyze practical issues of implementing layout of the new ISR.
- Analyze energy, delay and area overhead of the new ISR.
- Describe test chips.
- Conclusions.

Background: leakage currents (room temp)

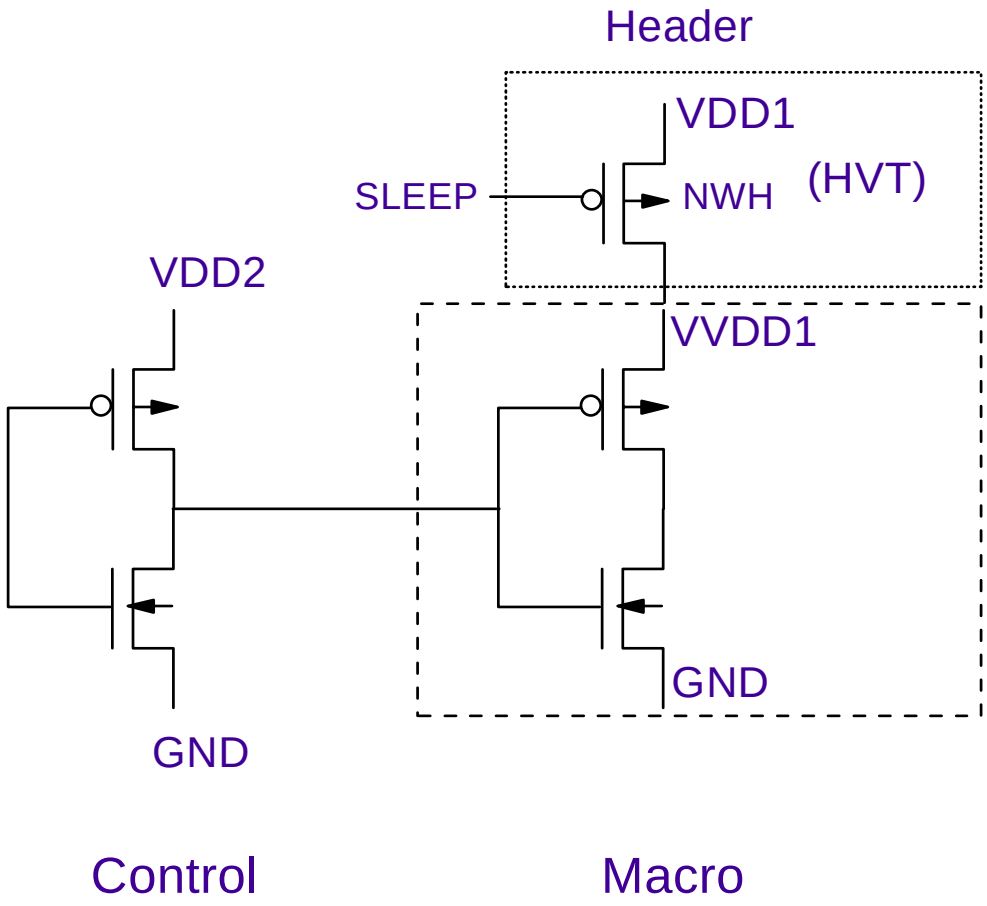


- Edward Nowak, “Maintaining the benefits of CMOS scaling when scaling bogs down”, IBM Journal of R&D, Vol. 46, No. 2/3, March/May 2002

Power down mode: system level



Background: MTCMOS



State saving alternatives 1

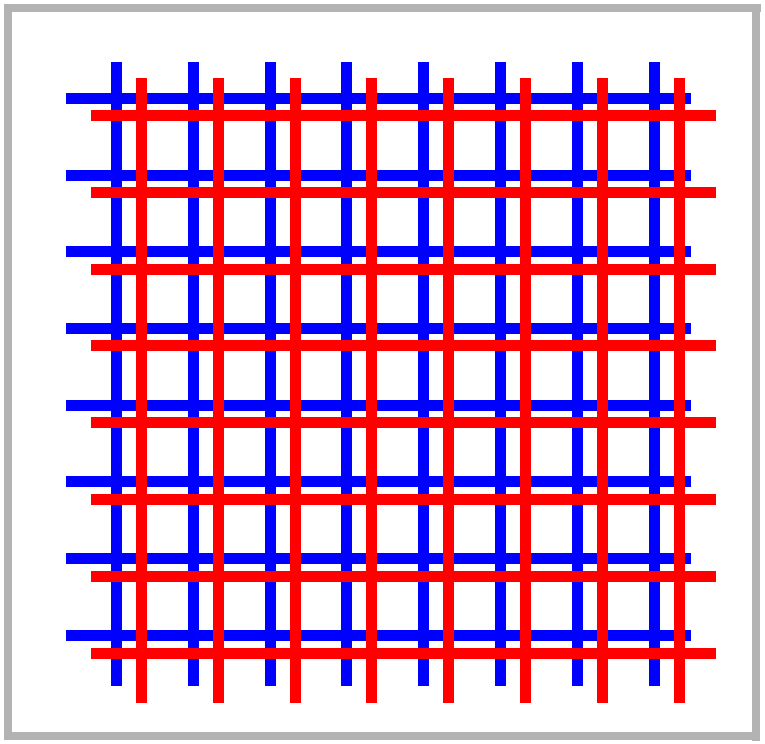
- Loose state, reboot on wake up
  - takes tens of seconds to wake up.
- Programmably save architected state to low-power local memory (SRAM / FLASH / DRAM), loose non-arch. state
  - OS call, high cycle overhead of saving and restoring the state,
  - high energy overhead (need to execute from tens to hundreds of instructions).
- Serially scan out the state, save it to a local memory
  - scan chain is part of the architecture - could cause design portability problems,
  - takes many cycles to save the state.
  - possible high energy overhead, high power during scan could be a problem too.

State saving alternatives 2

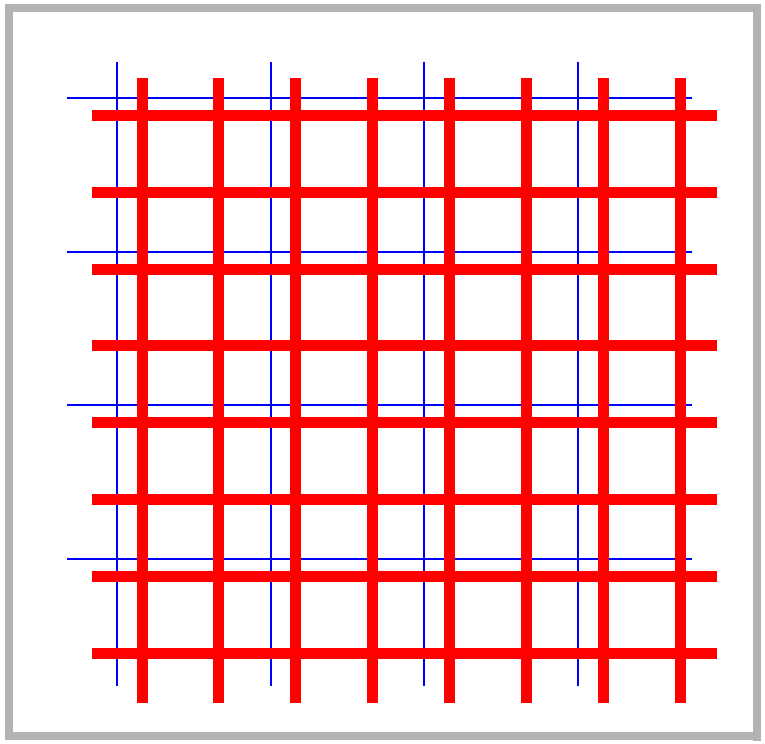
- Keep all latches on a separate power supply, power down logic
  - fast wake up, low energy overhead of saving the state, but
  - latches still leak (cannot use high Vt devices),
  - the additional supply feeds heavy current consumers,
  - have to pay the overhead of two full power supply distributions, or face
  - problems of dI/dt, noise, electromigration.
- Provide each latch with a shadow (called Retention Latch, RL), save state into RLs, keep RLs on a separate power supply
  - fast wake up, current consumption on the additional power supply is low,
  - overhead of the additional power supply distribution is low,
  - area and delay overhead, power overhead in the active mode.

External Power Gate Using Switchable DC/DC Converter

Dual High Current Supplies



Single High Current Supply

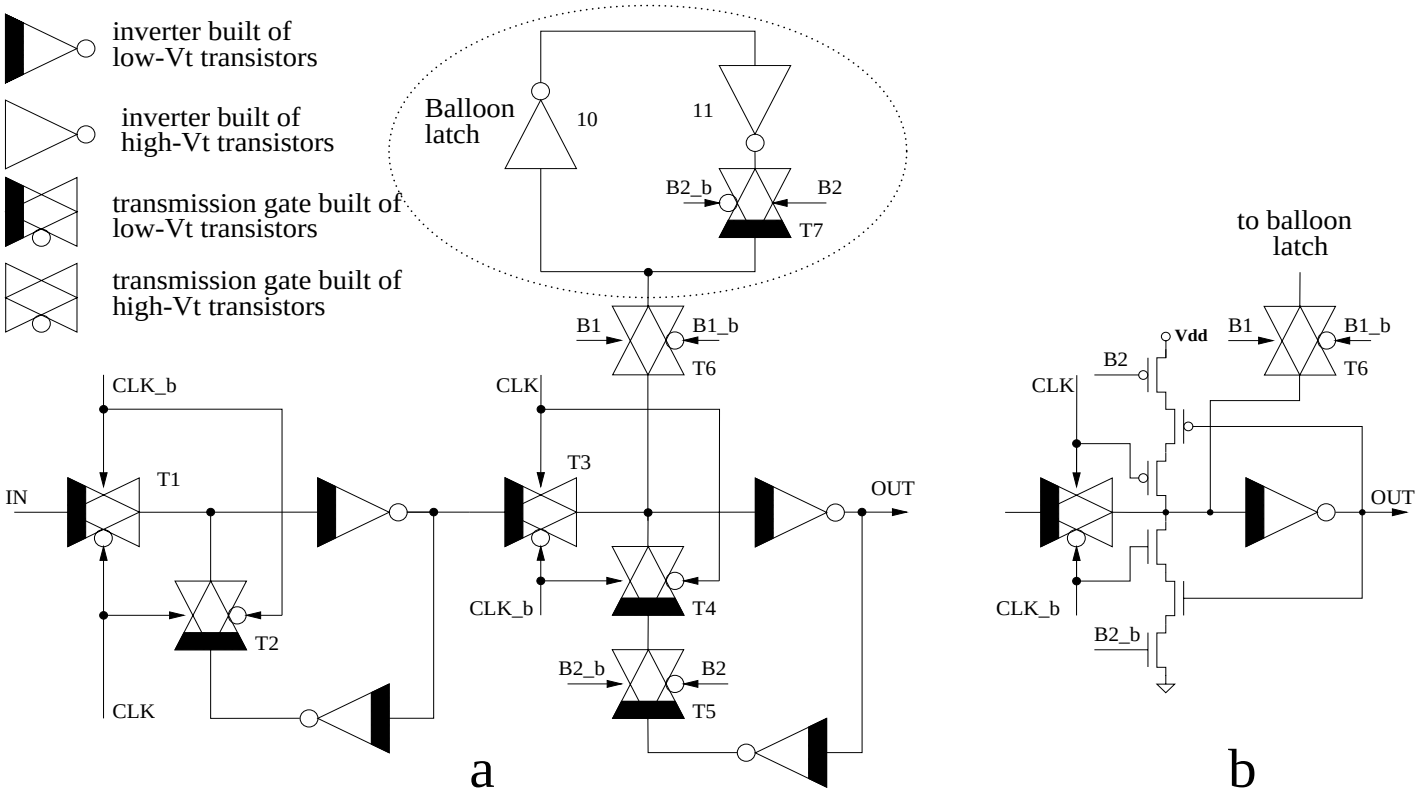


— VDD1

— VDD2

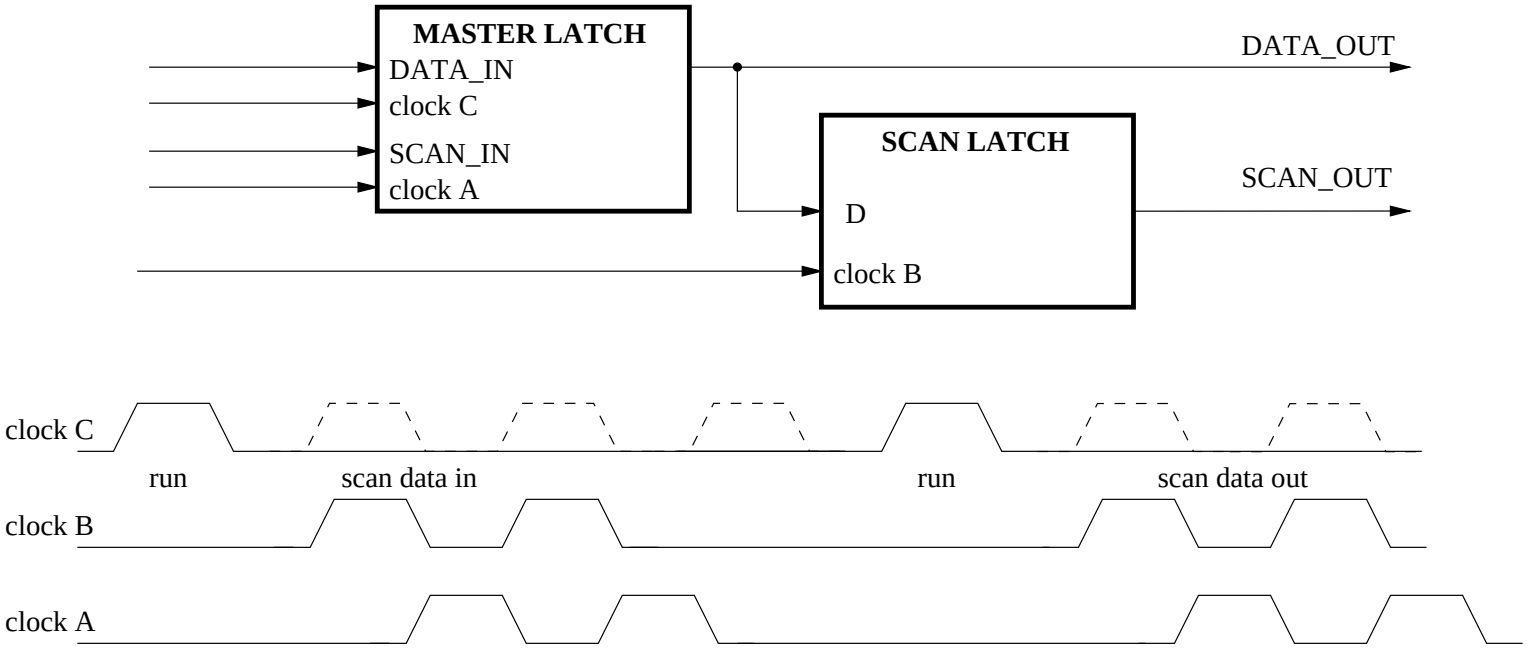
Prior art balloon latch

- $P_{RL\_overhead} = 0.5\ \alpha\ f\ V_{dd}^2\ C_b$ per latch in the active mode,
- $C_b = 6C_d + 2C_g + C_w$ (a) $C_b = 2C_d + C_w$ (b)
- power overhead is quite low, but what if scan mechanism is needed in addition to this?

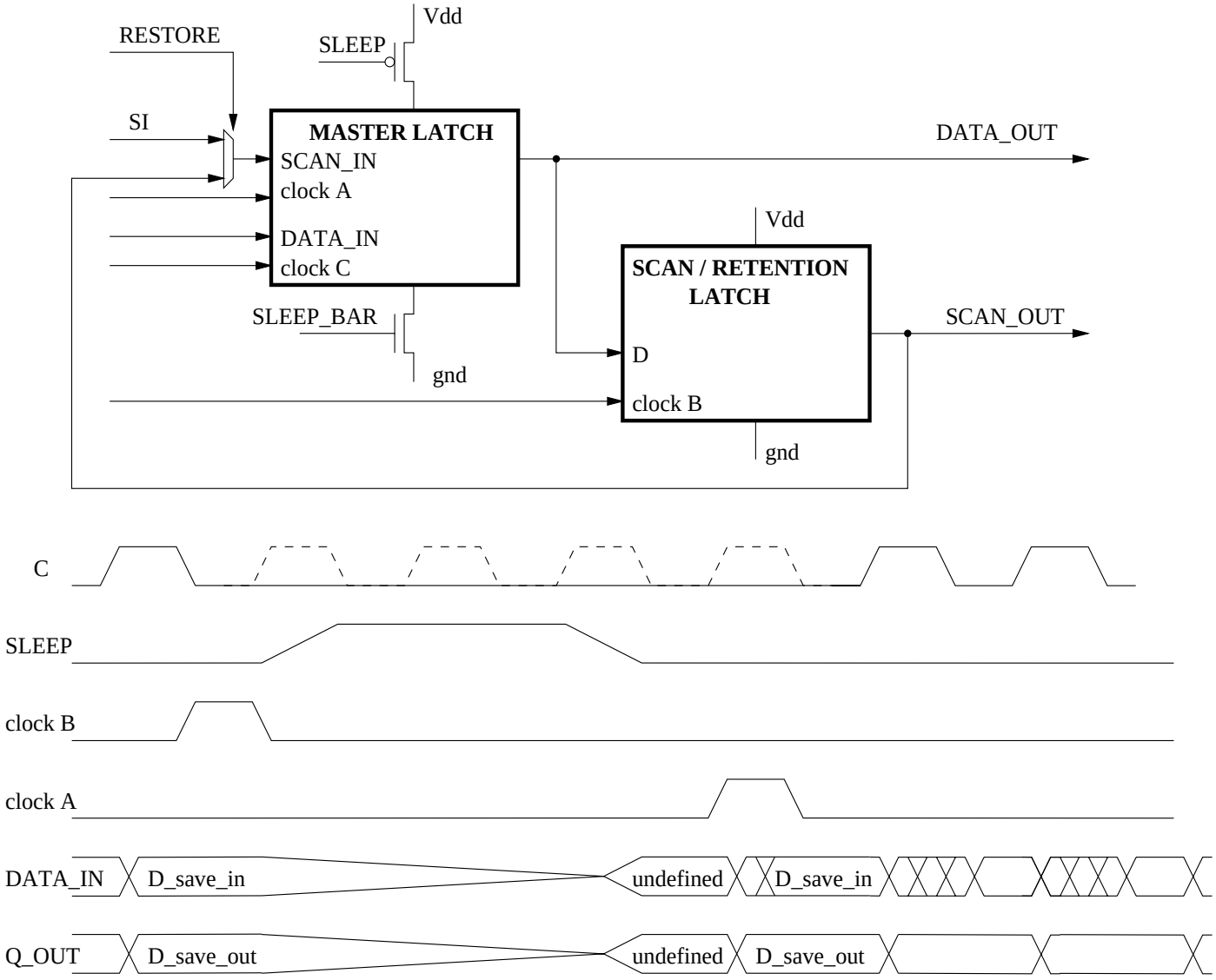


Prior art low-power scan mechanism

- $\mathbf{P_{scan\_overhead} = 0.5\ \alpha\ f\ V_{dd}^2\ C_s}$ per latch in the active mode,
- $\mathbf{C_s = 2C_d + 2C_g + C_{area}}$
- idea: reuse scan latch for data retention

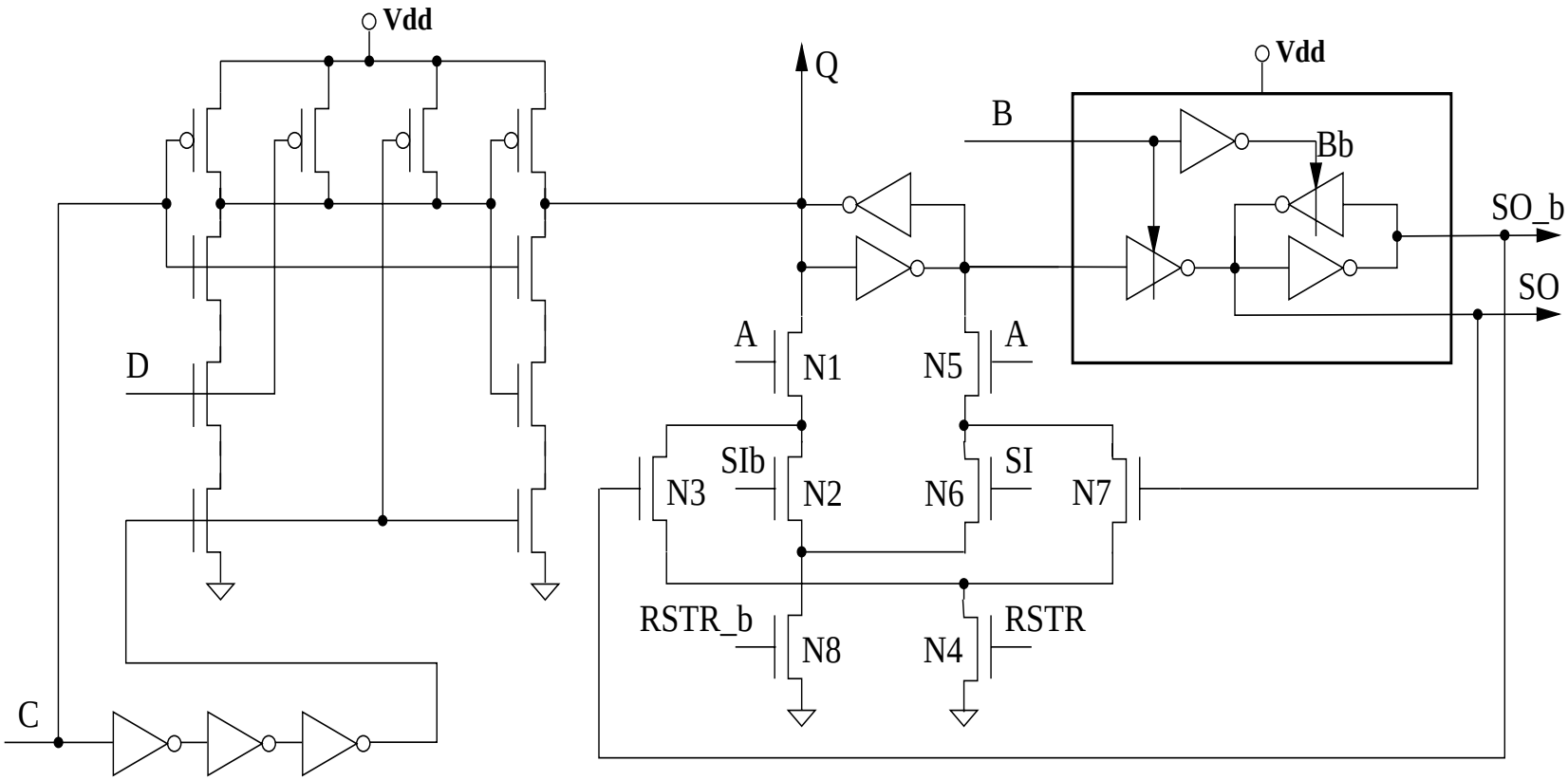


Integrated scan-retention mechanism

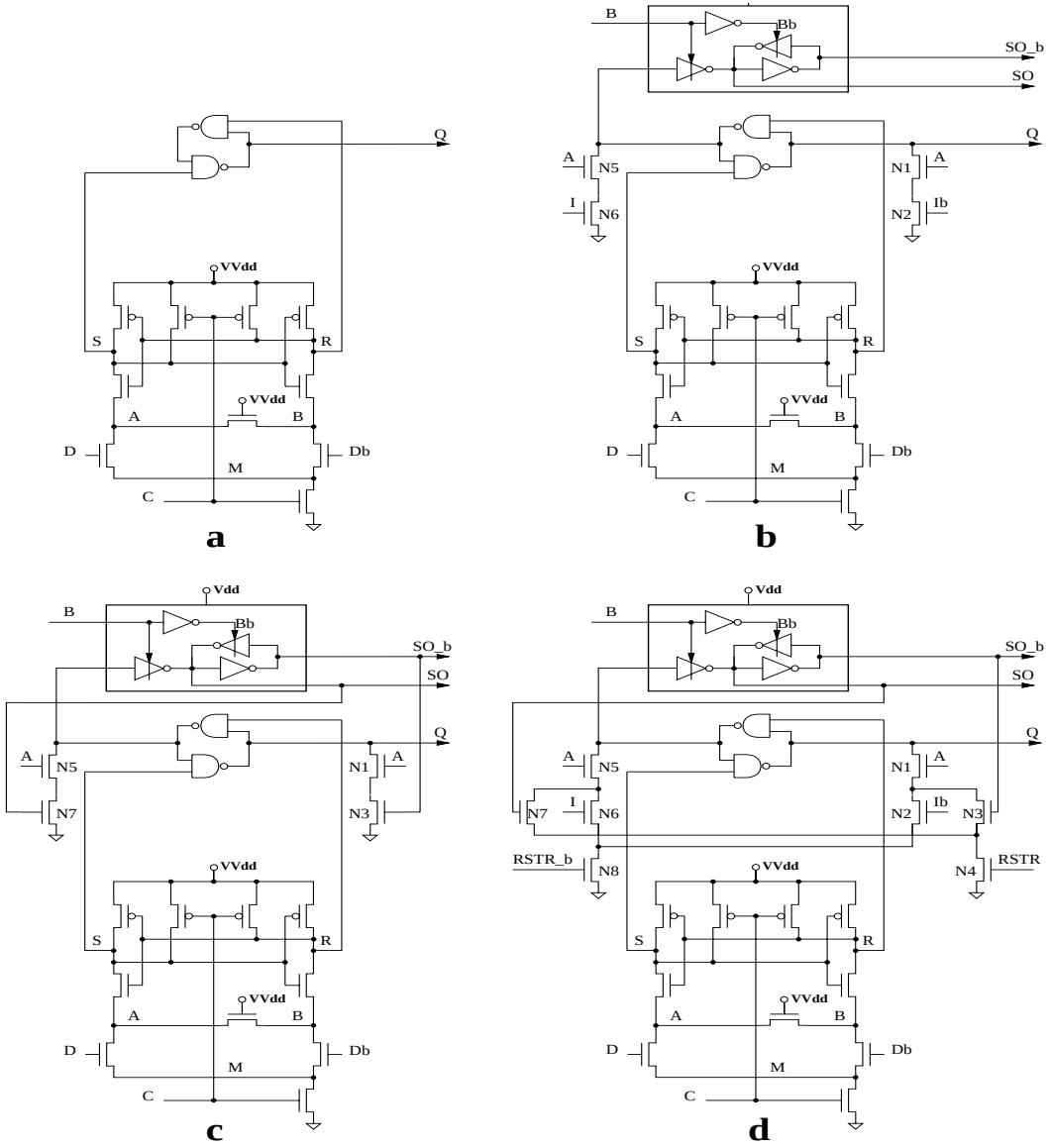


Scannable HLFF with data retention

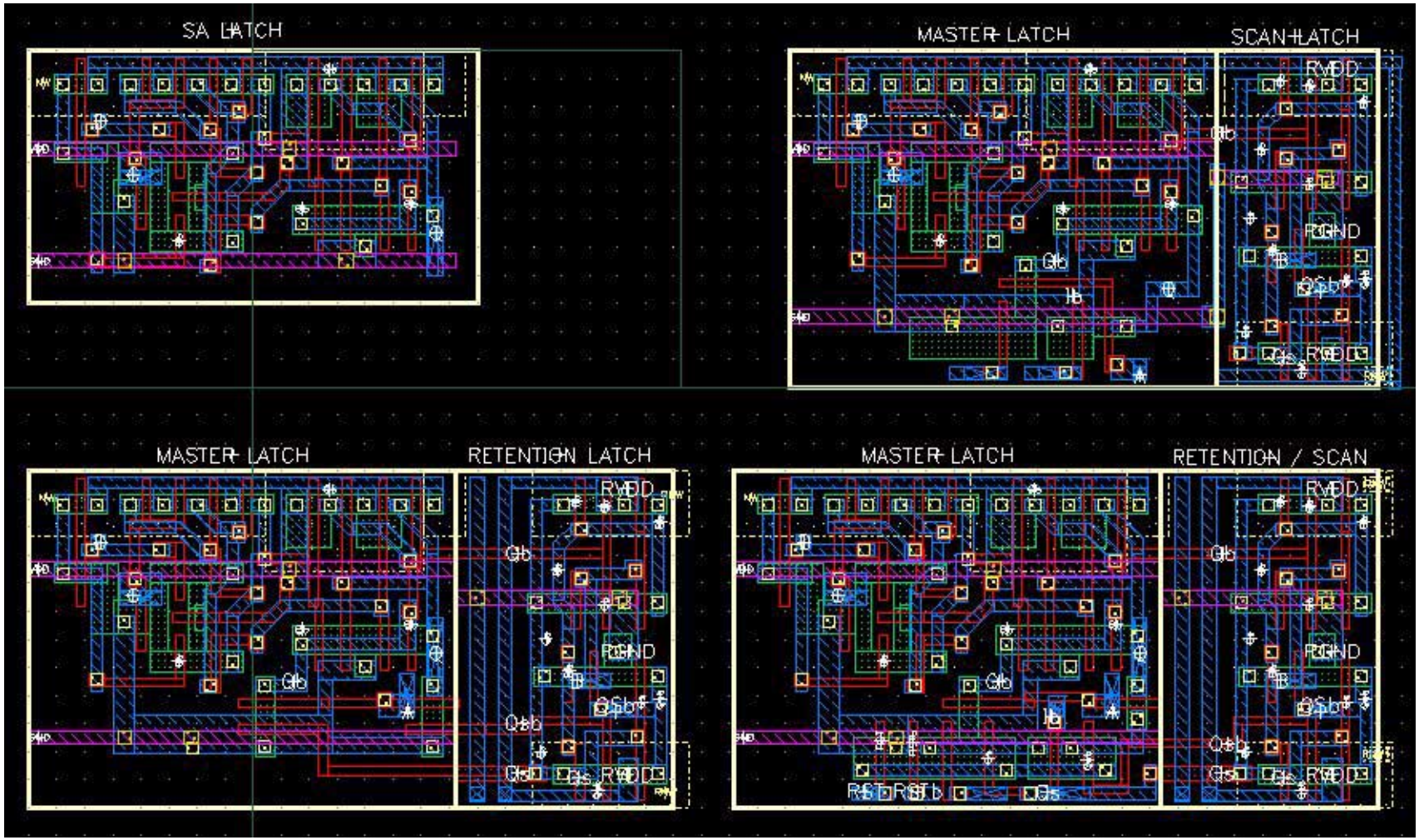
- $P_{ret\_scan\_overhead} = 0.5\ \alpha\ f\ V_{dd}^2\ C_s$ per latch in the active mode,
- $C_s = 2C_d + 2C_g + C_{area}$ (same overhead as scan without retention).



Scannable SA latch with data retention, schematic



Scannable SA latch with data retention, layouts

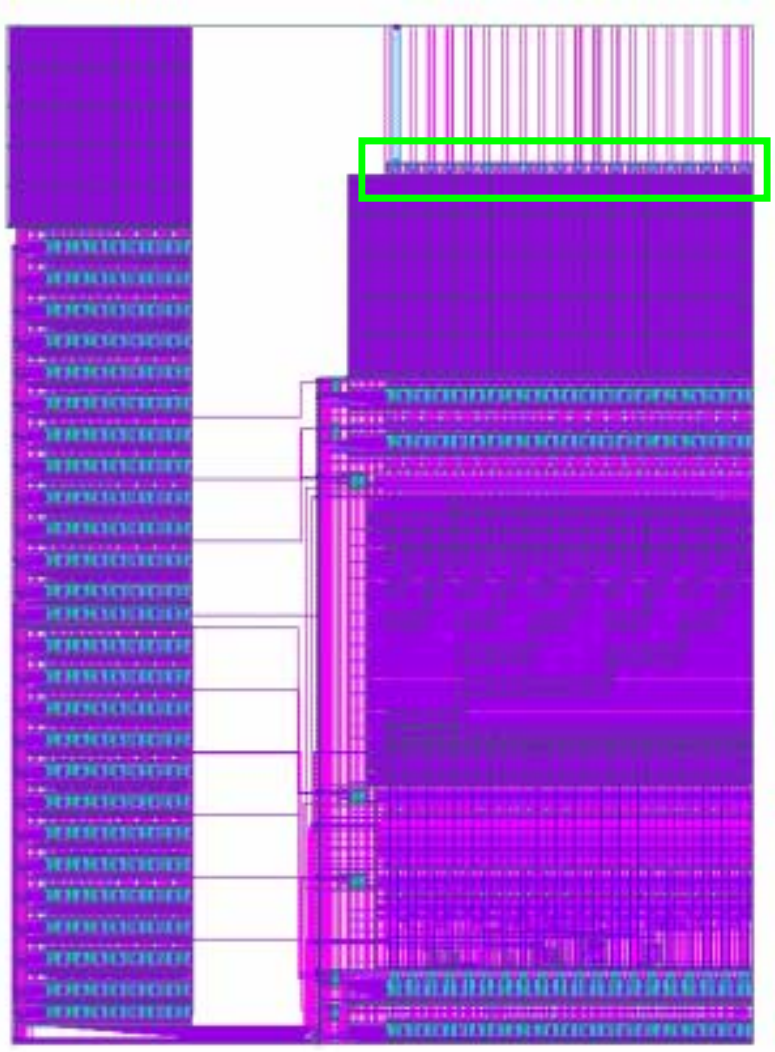


Comparison of the area, delay and power overhead

latch design	area		delay		energy	
	um^2	%	ns	%	fJ	%
- scan - retention (9tr)	**23.04**	**0**	**174**	**0**	**10.63**	**0**
- scan - retention (12tr)	**30.72**	**-**	**174**	**-**	**10.82**	**-**
+ scan - retention (12 tr)	**40.32**	**75 / 31**	**198**	**14**	**11.13**	**5 / 3**
- scan + retention (12 tr)	**44.16**	**92 / 44**	**200**	**15**	**11.15**	**5 / 3**
+ scan + retention (12 tr)	**44.16**	**92 / 44**	**200**	**15**	**11.15**	**5 / 3**

Based on simulations of netlists extracted from layouts of 16-bit registers.
Energy includes local clock distribution and overhead of the retiming latch.
Vdd = 0.9V.
switching factor α=0.3, average number of glitches per cycle β=0.16.

Test chip



VDD Decoupling Header Switch

2 x Retention Registers

Testing Control Registers

Adder

Logic

Comparator

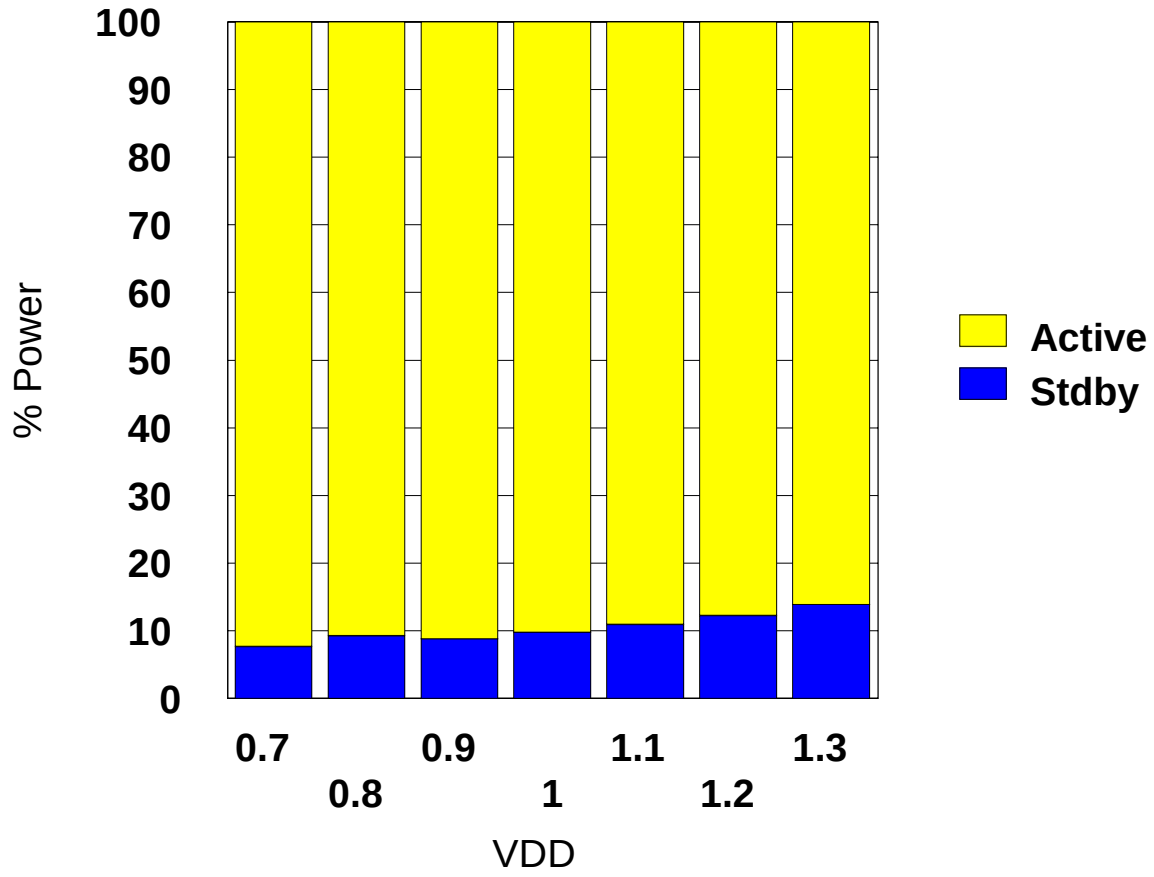
Retention Mux Register

MISR

0.13 um CMOS SOI Pipeline Testsite

Test chip measurements: active/standby power when PFET header is on (SOI, room temp)

- >20X reduction in standby power when header PFET is off



Conclusions

- Several approaches to saving state on power down compared.
- Retention latch approach is shown to have many advantages.
- Low energy integrated scan-retention mechanism proposed.
- Practical issues of implementing the new ISR discussed
- Energy, delay and area overhead of the new ISR analyzed.
- Experimental data measured on test chips in 0.13 CMOS SOI presented showing that
- >20x reduction in stand-by current achieved at a minimal active power overhead.