

Low Power SOC for IBM's PowerPC® Information Appliance Platform

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PowerPC®

IBM®

Power Efficiency Benefits Multiple Markets

New technologies that deliver high performance and greater power efficiency benefit a wide range of customers

- **Energy Constrained Wireless Devices**

- Web Pads
- PDAs
- Cell Phones
- Notebook PCs

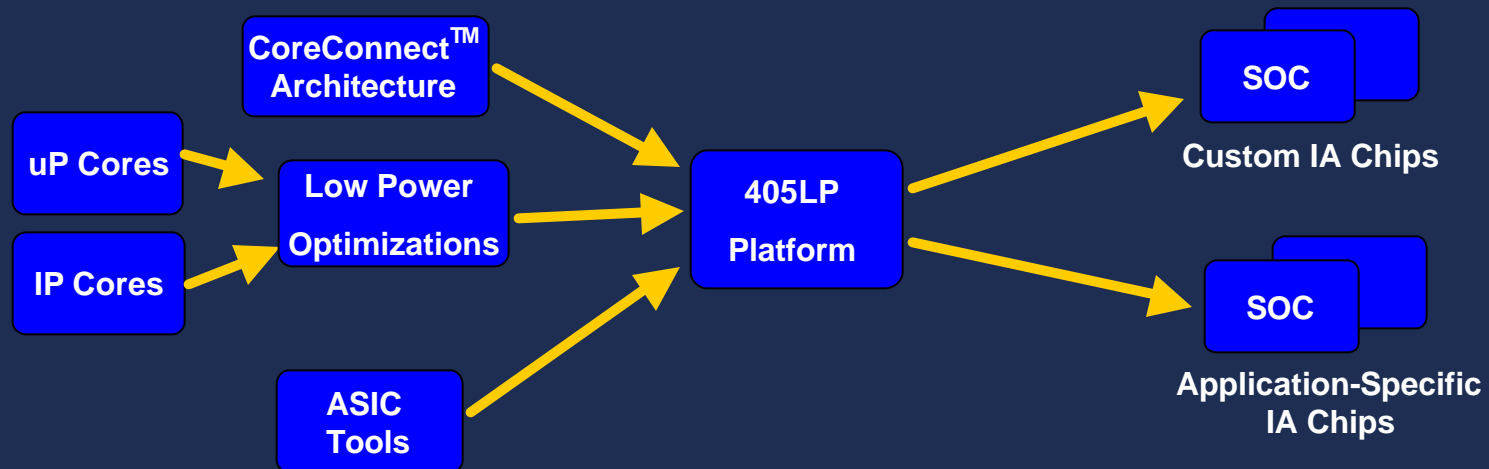
- **Power Sensitive Wired Devices**

- Cable/DSL Modems
- Routers/Switches
- Cellular Base Stations
- Line Cards

(power was never free and it's not getting cheaper)

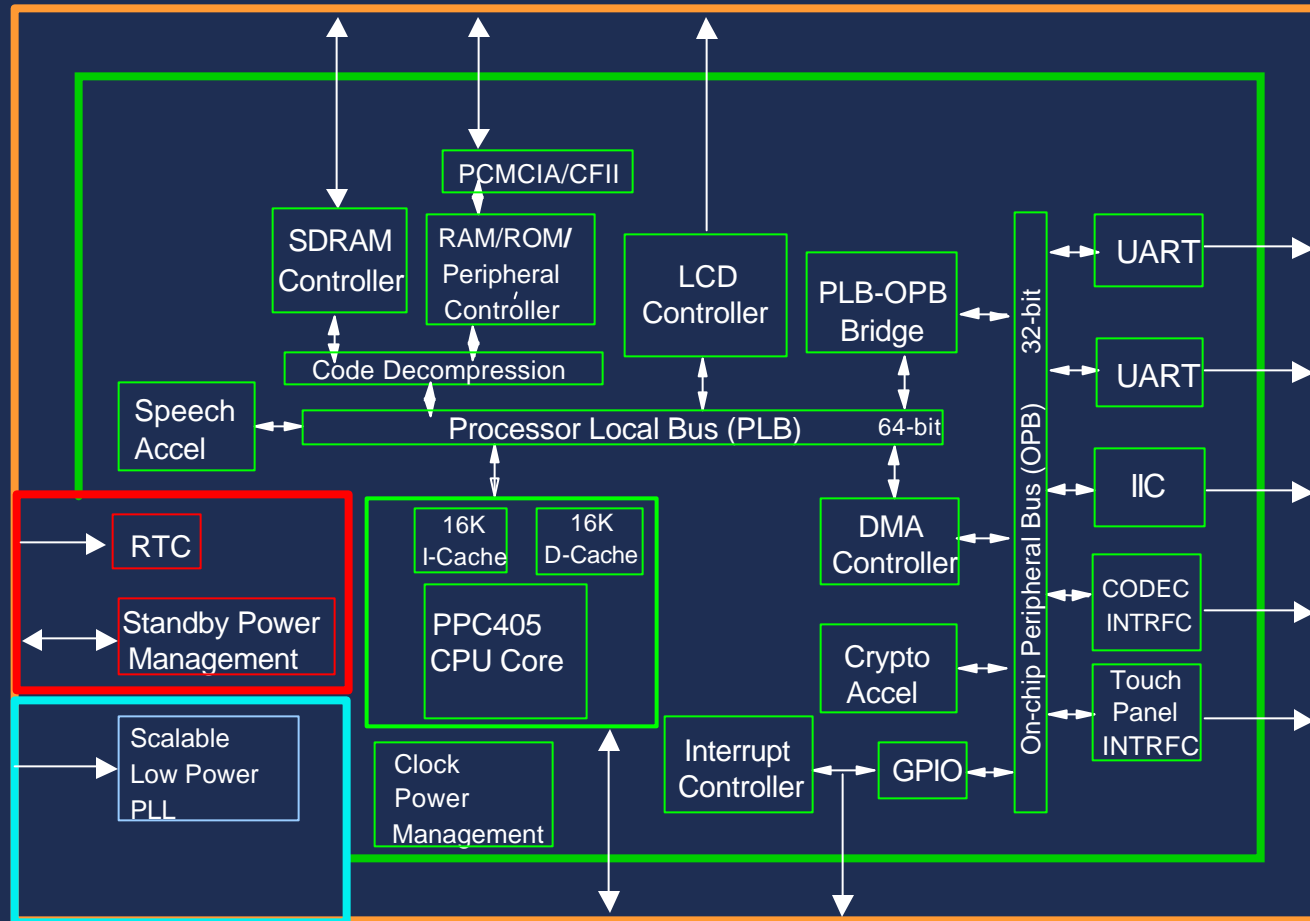
Platform for Information Appliances

405LP platform enables highly integrated, power efficient custom and application-specific Information Appliance (IA) chips



405LP System On a Chip

405LP integrates a rich set of functions for Information Appliances



Low Power Optimizations

The 405LP includes a wide range of low power optimizations to reduce both active and standby power

Active Power Reductions

- Voltage Scaling
- Frequency Scaling
- Flexible Clock Distribution
- Clock Gating
- Hardware Accelerators

Standby Power Reductions

- Clock Freezing
- Hibernation
- Voltage Reduction

Voltage Scaling in CMOS

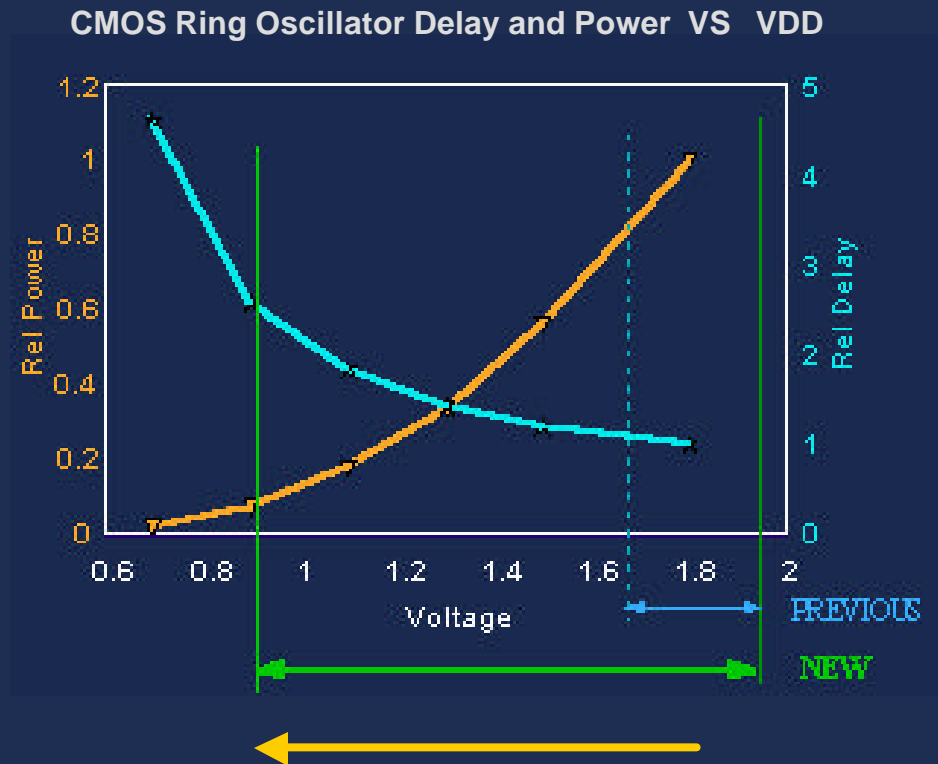
Reducing operating voltage greatly reduces active power in CMOS

Voltage Scaling Benefits

- Complementary CMOS scales well over a wide voltage range
- Can be used widely over entire chip
- Can optimize power/performance (MIPS / W) over a 4X range

Voltage Scaling Challenges

- Custom Circuits, PLLs, Analog, and I/O drivers don't voltage scale easily
- Avoiding increase standby power in low active power circuits
(the V_{TH} dilemma)



Operating at 1/2 normal Vdd increases delay 2.4-3.2X but reduces power by > 10X

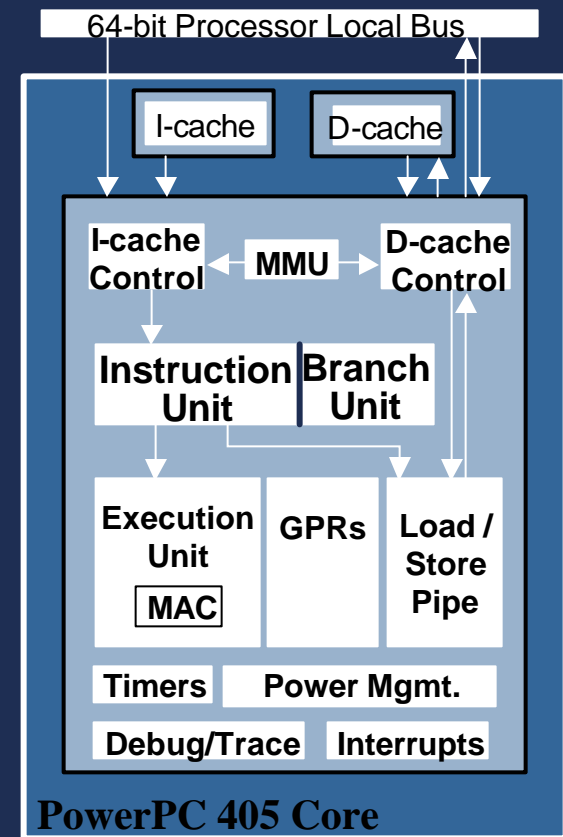
Scalable PowerPC 405 CPU Core

CPU Goals

- Expanded operating voltage range (0.9V to 1.95V)
- Maintain full software and tools with existing compatibility PowerPC 405
- Provide a high performance core capable of high efficiency low power operation

CPU Optimizations

- Redesigned custom circuits within CPU that were sensitive to low voltage operation
- Re-optimize design and timing for extended voltage range
- Verification of equivalence



Scalable Clock Generation Subsystem

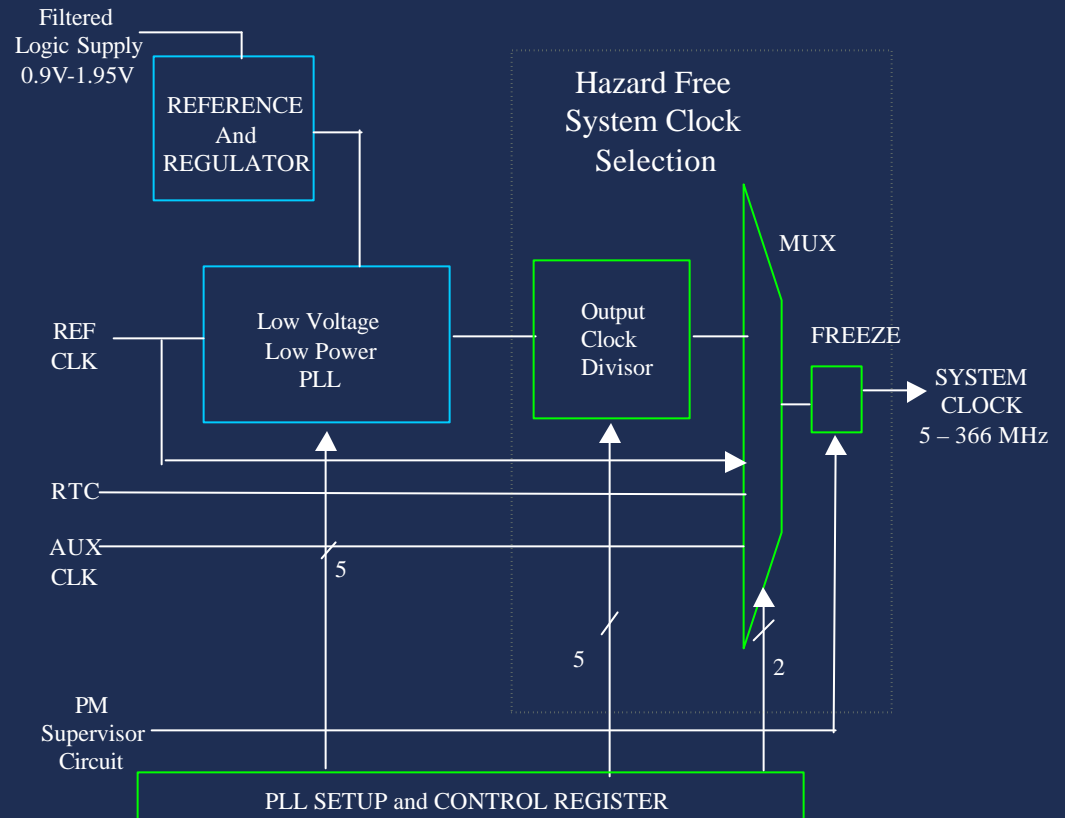
Clocking subsystem enables dynamic voltage and frequency scaling

Low Power Challenges

- Isolating PLL from effects of VDD scaling
- Enabling a wide range of input sources and output frequencies
- Level shifting and duty cycle correction

Clocking Subsystem Features

- Low voltage, low power PLL to generate a high frequency clock
- In-line self biasing regulator for dynamic VDD scaling
- Fast dynamic frequency scaling without losing PLL lock
- Hazard free system clock selection



Clock Domains and Clock Gating

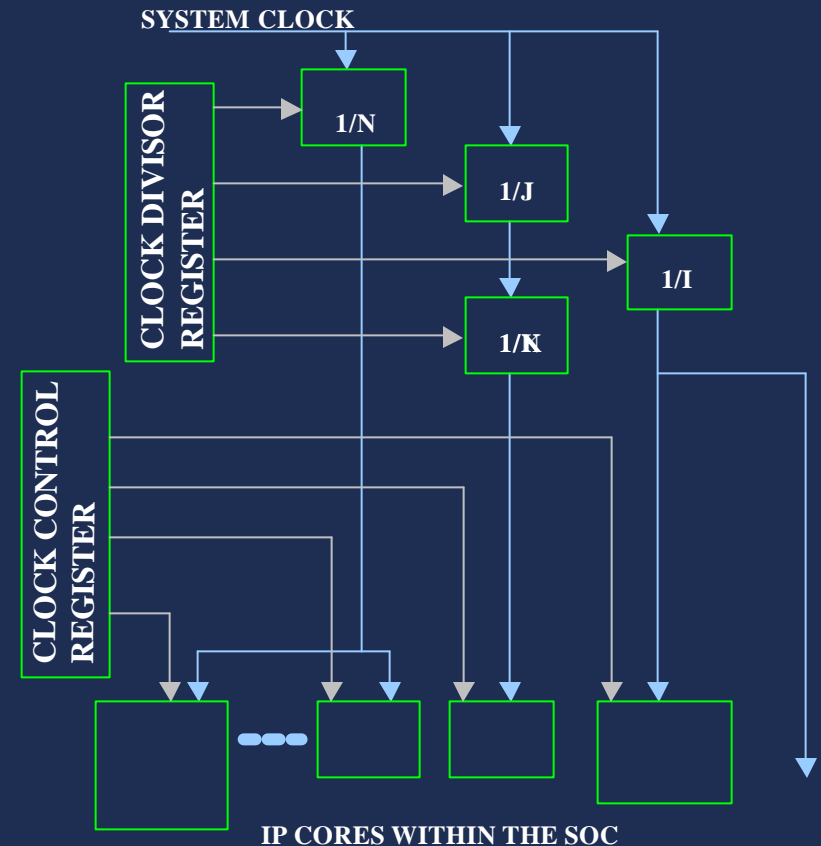
Clock distribution and clock gating used to reduce active power

Clock Domains

- On-chip clock distribution generates multiple synchronous phase aligned clock domains
- Support for dynamic frequency scaling via hazard free divisor selection

Clock Gating

- **IP core level** clock gating disables clocks to whole IP blocks that are not currently being used
- **Register level** clock gating disables clocks to unused portions of IP blocks during each operation or instruction cycle



Voltage Scalable Touch Panel Interface

New touch panel interface addresses unique low power challenges of analog sensor interfaces

Low Power Challenges

- Analog circuits do not benefit from CMOS voltage scaling
- Traditional A/D converters can be challenging to design at low VDD
- Protective voltage islands raise number of required supplies

Touch Panel Interface Features

- All digital CMOS solution based on an RC delay measurement
- Compatible with many standard resistive touch panels and other passive sensors
- Works over full logic voltage range
- Benefits of CMOS voltage scaling
- Provides up to 10-bits of resolution

Hardware Accelerators

Can increase performance or reduce overall active power

- Dedicated logic requires fewer cycles to execute algorithm than the main CPU
- Accelerators off load the CPU core allowing lower frequencies in both units
- Voltage scaling can be used in both hardware accelerator and CPU core

On-Chip Hardware Accelerators

Speech Language Accelerator

Targeted at embedded speech recognition software

Cryptography Accelerator

Supports DES and triple-DES encryption algorithms

CodePack™

Instruction compression to reduce system memory requirements

Active Power vs. Standby Power Tradeoffs

The V_{TH} Dilemma - Lowering the threshold voltage to reduce active power can increase standby/static power

Active Power

- Lower supply voltage significantly reduces active power ($p = C V_{dd}^2 F$)
- Threshold voltage limits the usable voltage range for complementary CMOS (V_{dd} / V_{TH})
- Lower threshold voltage (V_{TH}) allows a lower supply voltage and lower active power

Standby/Static Power

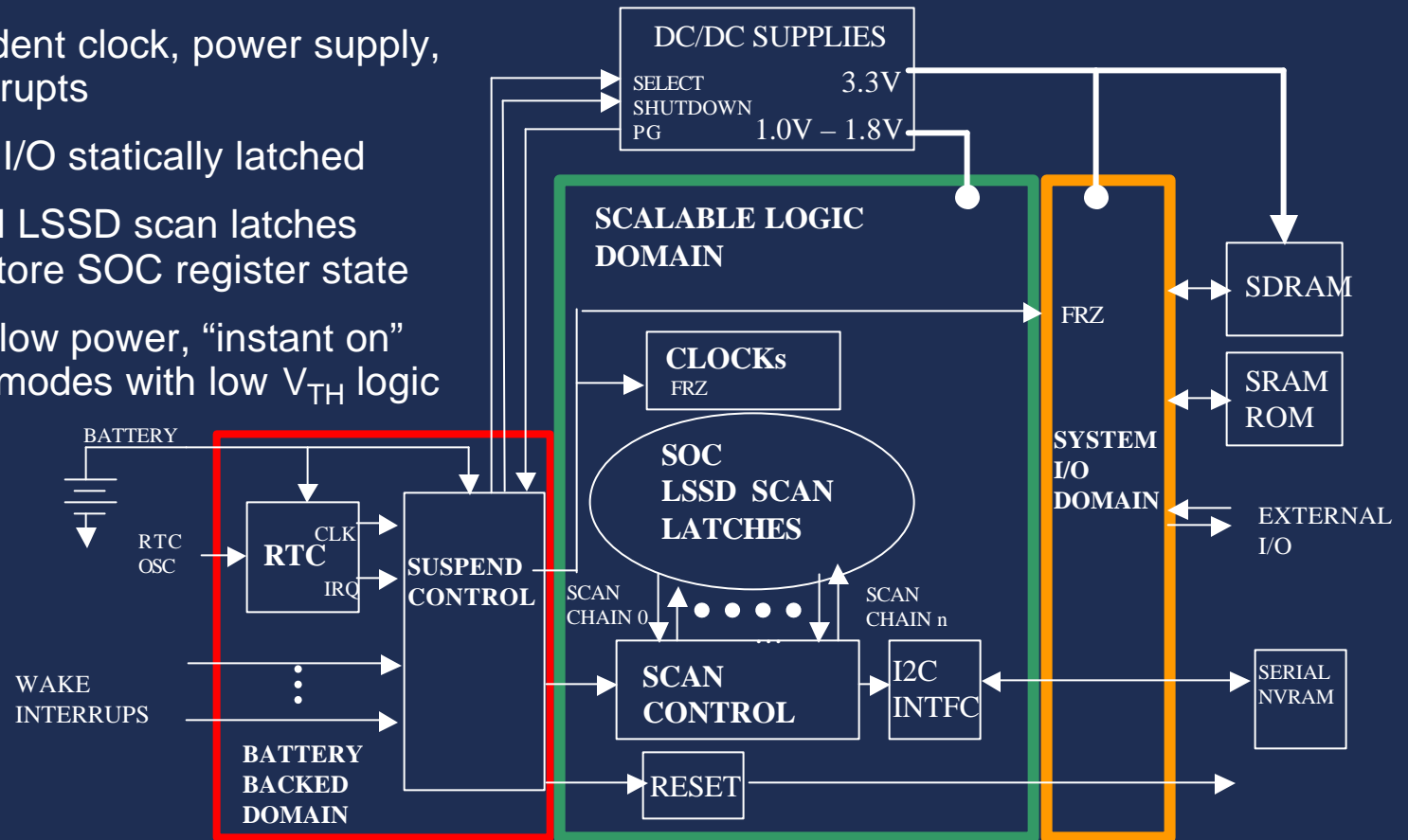
- Since devices are frequently idle, low standby power is important
- Higher threshold voltage (V_{TH}) reduces static leakage

Standby Power Reduction

On-chip supervisory core manages standby/static power

Features

- Independent clock, power supply, and interrupts
- External I/O statically latched
- Standard LSSD scan latches save/restore SOC register state
- Enables low power, “instant on” standby modes with low V_{TH} logic



Standby Power Modes

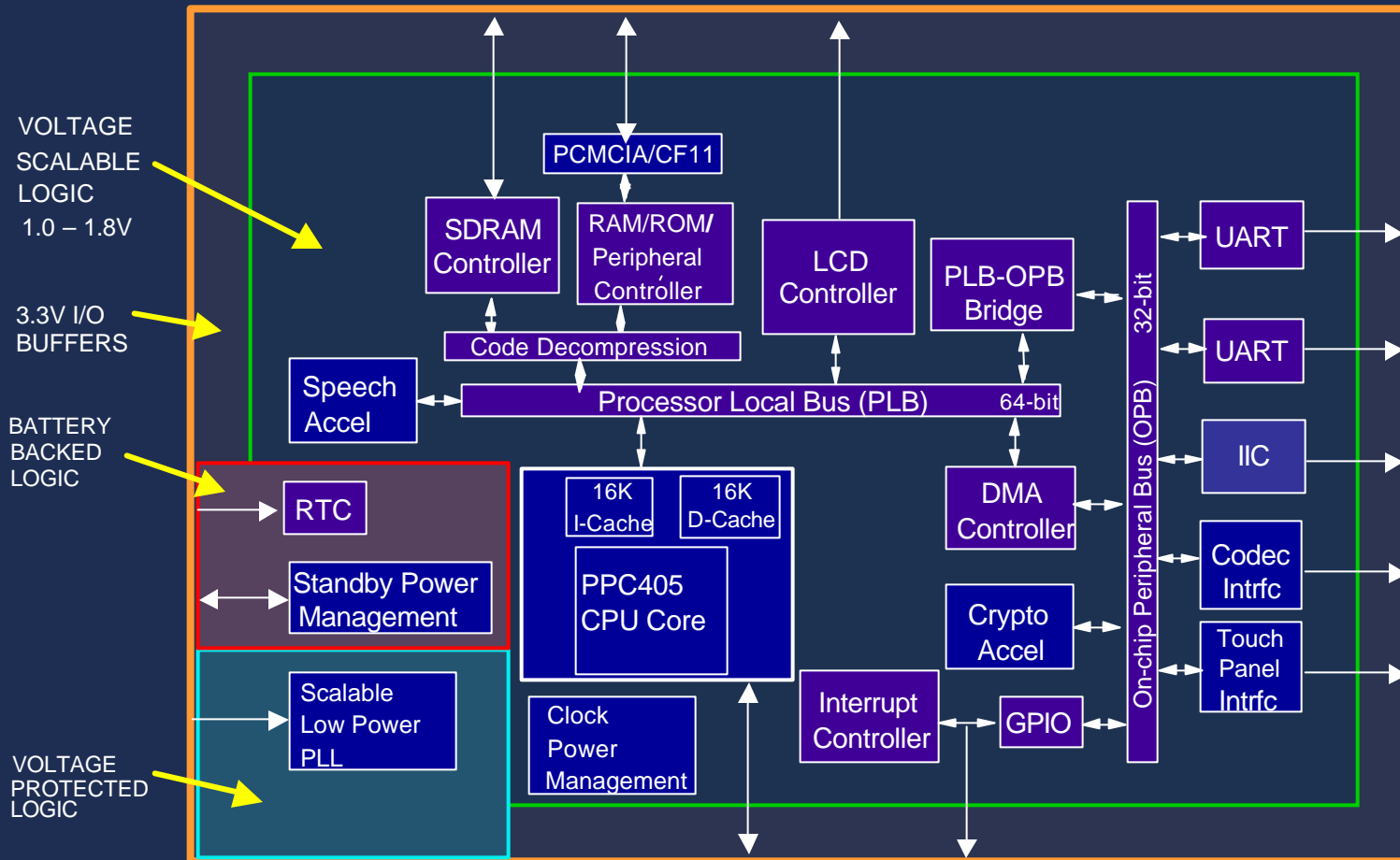
Standby power modes enable longer battery life and “instant on”

	System Clock	VDD Logic	State Saved	Restore Time	Power Logic
Freeze Mode	0 Hz	1V	All	Write DCR Register (< 1uS)	CMOS Leakage at 1V
Hibernation Mode	0	0	Software State	OS Reboot (Seconds)	~0
Cryo Mode	0	0	Registers and Software State	“Instant On” – Scan Restore of State (100- 200 mS)	~0

Cryo mode sequence

- Shutdown: Invalidate arrays → Clocks stopped → State scanned to IIC attached non-volatile storage → Power remove from logic
- Suspend: Monitor system for wake up condition or RTC timer
- Restore: On Wake indicator → Restore power to logic → State scanned in from non-volatile storage → Restore clocks

405LP Voltage Domains



CPU Core Specifications

Features

Architecture	32-bit PowerPC compliant, application code compatible with all IBM PowerPC processors
CPU/Caches	PPC405 16K I-Cache 16K D-Cache
Voltage	0.9V – 1.95V
Technology	0.18um, CMOS SA-27E

CPU Core/Caches Specifications

	TC1* (1.8V)	TC2* (1.0V)
Frequency	380 MHz	152 MHz
Performance (Dhrystone 2.1)	577 DMIPS	231 DMIPS
Typical Power (est.)	500 mW	53 mW
Performance/Watt	1154 DMIPS/ W	4528 DMIPS/ W

* Notes: TC1 – Typical Conditions: 1.8V, 55C, Nominal Silicon
TC2 – Typical Conditions: 1.0V, 55C, Nominal Silicon



What's Next?

- **Samples of 405LP SOC available to selected customers in 1Q '02**
- **Continuing innovation in low power techniques**
- **Developing highly integrated custom and standard SOC's based on these low power technologies**
- **For additional information:**
 - <http://www.chips.ibm.com/products/powerpc/>

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